

steps currently used to create back contact cells, while maintaining the high solar cell efficiencies. Currently, the only commercial seller of back contact solar cells is Sunpower, which has an expensive and many-step process to make solar cells. The current commercial process used to process back contact solar cells involves at least twenty steps and has a cost of approximately \$0.80/Wp. The process of the present invention requires fewer steps and dramatically reduces the cost to approximately \$0.25/Wp.

[0099] The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be readily apparent to one skilled in the art that other various modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention as defined by the claims.

What is claimed is:

1. A solar cell comprising:
 - a semiconducting wafer having a front surface, a back surface, and a background doped region between the front surface and the back surface;
 - a front alternatingly-doped region extending from the front surface of the semiconducting wafer to a location between the front surface and the back surface, wherein the front doped region comprises laterally alternating first front doped regions and second front doped regions, the second front doped regions having a lower sheet resistance than the first front doped regions, and wherein a p-n junction is formed between the first front doped regions and the background doped region;
 - a plurality of front metal contacts aligned over the second front doped regions, wherein the front metal contacts are configured to conduct electrical charge from the second front doped regions;
 - a back alternatingly-doped region extending from the back surface of the semiconducting wafer to a location between the back surface and the front surface, wherein the back doped region comprises laterally alternating first back doped regions and second back doped regions, the second back doped regions having a lower sheet resistance than the first back doped regions; and
 - a back metal contact layer disposed on the back surface of the semiconducting wafer, wherein the back metal contact layer covers the first back doped regions and the second back doped regions and is configured to conduct electrical charge from the second back doped regions.
2. The solar cell of claim 1, wherein the semiconducting wafer is a silicon substrate.
3. The solar cell of claim 1, wherein the first front doped regions and the first back doped regions have a sheet resistance between approximately 80 Ohms/square and approximately 160 Ohms/square.
4. The solar cell of claim 1, wherein the second front doped regions and the second back doped regions have a sheet resistance between approximately 10 Ohms/square and approximately 40 Ohms/square.
5. The solar cell of claim 1, wherein:
 - the first front doped regions and the first back doped regions have a sheet resistance between approximately 80 Ohms/square and approximately 160 Ohms/square; and

the second front doped regions and the second back doped regions have a sheet resistance between approximately 10 Ohms/square and approximately 40 Ohms/square.

6. The solar cell of claim 5, wherein the background doped region has a sheet resistance between approximately 0.5 Ohms/square and approximately 1.5 Ohms/square.

7. The solar cell of claim 1, further comprising an anti-reflective coating layer disposed on the front surface of the semiconducting wafer over the first front doped regions.

8. The solar cell of claim 1, further comprising a metallic seed layer disposed over the second front doped regions and under the front metal contacts.

9. The solar cell of claim 8, wherein the metallic seed layer comprises mesotaxy implants.

10. The solar cell of claim 8, wherein the metallic seed layer comprises a silicide.

11. The solar cell of claim 1, wherein the second front doped regions are laterally spaced apart from one another a distance in the range of approximately 1 mm to approximately 3 mm.

12. The solar cell of claim 1, wherein:

the background doped region is p-type doped; and
the first front doped regions and the second front doped regions are n-type doped.

13. The solar cell of claim 12, wherein the second back doped regions are doped with the same charge-type dopant as the background doped region.

14. The solar cell of claim 13, wherein the first back doped regions are doped with the same charge-type dopant as the second back doped regions and the background doped region.

15. The solar cell of claim 13, wherein the second back doped regions and the background doped region are p-type doped.

16. The solar cell of claim 15, wherein the second back doped regions are doped with boron.

17. A method of fabricating a solar cell, the method comprising:

providing a semiconducting wafer having a front surface, a back surface, and a background doped region between the front surface and the back surface;

performing a first set of ion implantations of dopant into the semiconducting wafer to form a front alternatingly-doped region extending from the front surface of the semiconducting wafer to a location between the front surface and the back surface, wherein the front doped region comprises laterally alternating first front doped regions and second front doped regions, the second front doped regions having a lower sheet resistance than the first front doped regions, and wherein a p-n junction is formed between the first front doped regions and the background doped region;

disposing a plurality of front metal contacts on the semiconducting wafer, wherein the front metal contacts are aligned over the second front doped regions and are configured to conduct electrical charge from the second front doped regions;

performing a second set of ion implantations of dopant into the semiconducting wafer to form a back alternatingly-doped region extending from the back surface of the semiconducting wafer to a location between the back surface and the front surface, wherein the back doped region comprises laterally alternating first back doped regions and second back doped regions, the second back