

[0124] Referring to FIG. 2I, with the common voltage (V_{COM}) high, the actual video signal is scanned into the matrix circuit. After a delay to allow for the liquid crystal to twist into position, the LED backlight 1111 is flashed to present the image. Prior to the next screen or subframe, a heat cycle occurs where all the row lines are driven such that there is a voltage differential across the row. The heating can occur while V_{COM} and the video are being alternated and inverted, respectively, by the frame control line 1131. FIG. 2I shows a heating cycle after each subframe, but the number and time period of heat cycles can be dependent on the temperature of the liquid crystal as determined by the temperature sensor 1132. In cold environments, the digital circuit 1120 can have a warm-up cycle where the heater is turned on prior to the first painting of the screen.

[0125] Still referring to FIG. 2I, driving V_{COM} low erases the image that has just been scanned. However, since there is no backlight on, the erasure of the image is not seen. With V_{COM} low, the inverted video signal is scanned into the matrix circuit. Similarly after a delay to allow the liquid crystal to twist, the LED backlight 1111 is flashed to present the refreshed or new image. Prior to the next screen, frame 1, subframe 3 in the Figure, V_{COM} goes high. The driving V_{COM} high results in the image that has just been scanned to be destroyed. With V_{COM} high, an actual video signal is scanned into the matrix circuit. A delay occurs and then the LED backlight 1111 is flashed. The common voltage (V_{COM}) and the video keep on alternating.

[0126] The delay time before beginning the flash and the flash time are shown as identical in FIG. 2I. However, both the delay time (the delay for response time of the liquid crystal) and the flash time can be dependent on the specific color to be flashed. The delay time is dependent on when the liquid crystal associated with the last pixel to be written has sufficient time to twist to allow that specific color to be seen. The duration of the flash, or the point that the flash must be terminated, is dependent on when the liquid crystal associated with the first pixel to be written of the next frame has twisted sufficiently that light from the backlight is visible to the viewer. For example referring to FIG. 2I, it is not desirable for the red flash to be on, when the writing for the blue subframe has progressed to the point that the first pixel written for the blue subframe has resulted in the liquid crystal being optically transmissive for red wavelengths. The ending of the flash does not have to occur until sometime after the beginning of the writing of the next subframe because of response time of the liquid crystal.

[0127] The timing control circuit 1122, as seen in FIG. 2F, can vary the flash duration and the delay or response time dependent on the color that is to be flashed. In addition, the current to the backlights 1111 can be varied to adjust the intensity of the color. If desired, a color control line 1127 can be added to the timing control circuit 1122 to allow the user to vary the color.

[0128] It is recognized that the method of generating heat is different on different displays. For example, referring to FIG. 2A in which a select scanner 46a and 46b is located on both sides of the display and is connected to each end of the row, in typical operations either both ends are high or both ends are low depending on whether the row is being addressed. In order to heat the display, one of the select scanners, for example 46a, can be driven high for all the

rows, and the other select scanner, for example 46b, is driven low for all rows therein creating a voltage difference across the row lines.

[0129] The clock timing sent to the display 1112 is shown in FIG. 2I. The clock timing is needed by the display 1112 only when writing to the pixels. The capacitance of the storage capacitor holds the liquid crystal in the proper position during the time the backlight 1111 is flashing. By periodically sending clock signals to the display 1112 for typically as much as fifty percent (50%) of the total time or less results in a power reduction.

[0130] Referring to FIG. 2J, a schematic of the display 1112 and the digital to analog converter 1130 are shown. The display has a horizontal shift register 1136, a vertical shift register 1142, and switches 1140 similar to what is illustrated in FIG. 2H. In addition, and in contrast to FIG. 2H, FIG. 2J illustrates a heating gate 1154.

[0131] Referring to FIG. 2K, for pixels which have p-channel TFTs, the heating gate 1154 has a series of n-channel TFTs. Typically when writing to the display only the row being written to is on ($V=0$). When not writing to the display, all the rows are V_{DD} . When the n-channel TFTs turned on, by applying V_{DD} to a heat line 1150 results in current flowing from the inverter associated with the vertical shift register 1142 through the row to the n-channel TFT and heat is dissipated along the entire row. The drain is connected to V_{EE} , which is zero. It is also recognized that the display 1112 can have several extra rows outside the typical array to assist in uniform heating.

[0132] Likewise for pixels which have n-channel TFTs, referring to FIG. 2L the heating gate 1154 has a series of p-channel TFTs. Typically when writing to the display only the row being written to is on ($V=V_{DD}$). When not writing to the display, all the rows are approximately zero (0) volts. When the p-channel TFTs are turned, by setting the gate to zero (0), there is a voltage drop across the row of V_{DD} .

[0133] It is recognized that V_{COM} addressing and the heating of the display can be used independently. Heating can be incorporated into the embodiments described with respect to FIGS. 2A-2D. While an internal heater is preferred, it is recognized that a separate heater can be used with the temperature sensor.

[0134] Referring to FIG. 2M, a sectional view of the display 1112 is shown. The display 1112 has an active matrix portion 1160 including a pixel element 2047 spaced from a counterelectrode 2085 by an interposed liquid crystal material 2080. Each pixel element 2047 has a transistor 2054 and a pixel electrode 2065. The active matrix portion 1160 can have aluminum light shields 2086 to protect the transistor (TFT) 2054 if the active matrix is used for projection requiring high luminance light. The counterelectrode 2085 is connected to the rest of the circuit by solder bumps 2088. The matrix 1160 is bounded by a pair of glass substrates 2090 in this embodiment and a pair of polarizers 1162. An additional pair of glass plates 1164 are located outboard of the active matrix portion 1160. The glass plates 1164 are spaced from the polarizer 1162. The space defines an insulation layer 1166. The display 1112 includes a two-piece case 1168 which contains the active matrix portion 1160, the glass plates 1162 and the polarizers 1164. A room temperature vulcanization (RTV) rubber 1170 helps in maintaining the elements in proper position in the case.