ments or buttons on a control panel **774** of the reader housing **768** to operate the system. The elements can include an on/off switch **778** and a four way element to scroll the display up, down, left or right.

[**0244**] The card reader system can be used to access or change the data stored on the card or select an option from choices provided through a PCMCIA modem. The user can change the data or make the selection using a four way element **710** and a select button **716**, such as shown in **FIG. 17A**.

[**0245**] **FIGS. 19C***a*-**19C***b* discloses a schematic of an embodiment of a circuit **780** for the card **730**. The circuit **780** has a control chip **782**, a memory chip **784**, and an interface chip (flashcard) **786**. The control chip **782** takes the images stored on the memory chip **784** and sends the signal to the interface chip **786**. The control chip **782** and the memory chip **784** are connected by both address lines **788** and data lines **790**. In addition, an output enable (OE) line **792** extends between the control chip and the memory chip to allow the card **730** both to be read and to store data. The control chip **782** takes the image and sends the image in a series of bits to the interface chip **786**.

[**0246**] The interface chip **786** has eight connection points **794**, **796**, **798**, **800**, **802**, **804**, **806**, and **808** for interacting with an interface connection **816**, as illustrated in **FIG. 19**D, on the card reader **750**. The card **730** receives power (voltage) and is grounded through the connections **794** and **796** made on the interface chip **786**. The card receives a frame reset signal through a frame reset connection **798** to allow the control chip **782** to know when to send the next frame. A picture increment signal sent through a picture increment connection **800** allows the control chip **782**-to shift addresses to another stored picture. A clock signal to the control chip from the clock connection **802** regulates the flow of data. The control chip **782** sends a bit of data for each clock pulse and waits for a signal before starting the next row. The image signal is sent from the memory **784** through the control chip **782** to a data out connection **804** to the card reader **750**.

[**0247**] The mode input **806** is used to switch between a read and a write mode. The data in connection **808** is for writing data to the memory.

[**0248**] **FIGS. 19D, 19E***a*, and **19E***b* illustrate a schematic of a display control circuitry **810** in the card reader **750**. The display control circuit **810** has a battery, which through a digital power supply **812** and an analog power supply **814**, powers the circuit **810** as represented in **FIG. 19D**. The flash connection **816** of the card reader **750** is the interface with the flashcard **786** of the card **730**. The flash connection **816** sends the signals and power described above including the clock, the frame reset and picture increment from a control chip **820**. The control chip **820** receives its clock signal from a 20 MHz clock chip **824**. The picture increment is set high by a switch **826**, which is physical connected to a button on the control panel **774** of the reader housing **768**.

[**0249**] The data signal from the card **730** through the flash connection **816** is sent to a switch circuit **830** which set the signal high (V_{DD}) or low (V_{COM}) depending if the signal is a high bit (1) or a low bit (0). The video signal is sent from the switch to a connector, which connects to the microdisplay. The connector in addition send the control signals from the control circuit and power to the microdisplay. The LEDs for the backlight are controlled each by a transistor and a signal from the control chip.

[**0250**] The circuit in addition has a power down reset circuit. The power down reset circuit sends a signal to the microdisplay to clear the image before the power is off.

[**0251**] **FIGS. 19D, 19E***a*, and **19E***b* represent a 1 bit color display control circuit which displays eight colors (red, blue, green, black, white, magenta, cyan, and yellow). By selecting varying voltages between V_{EE} and V_{DD} as illustrated in **FIG. 19**F and having two switches, a 2 bit color display control circuit having 64 colors is possible. It is recognized that greater number of colors are desired, but for items such as pagers and cellular telephones, the wireless transmission rate may limit the bits available for transmitting image data. With these limited transmission rates the available number of colors for displayed is reduced until better compression systems and transmission rates are available. With limited colors because of transmission rates, a switch chip is preferred to a video processor because of power requirements. For items such as cameras and other products not including wireless transmission 8 bit color displays having 16 million colors is preferred.

[**0252**] The display module shown in **FIG. 19B** can be equipped with an antenna and television receiver to provide a pocket size color television.

[**0253**] Head Mounted Display System

[**0254**] In yet another embodiment of the invention shown in **FIG. 20**A, the HDTV color active matrix display, as described in connection with **FIG. 2**A, is provided with suitable optics and incorporated into a housing **860** and pivotally attached to a headband frame **861** to provide a novel head mounted display system **864**. In general, the system **864** is comprised of a unique headband frame **861** and adjustable strap **862** for attaching the system to the user's head, a side-mounted speaker system **866** connected by cable **868** to electronics console **870** attached to the front of the frame **862**, a microphone **872** rotatably suspended from speaker frame **874**, and the aforementioned display housing **860** dependent from console **870** and electronically connected thereto by cable **876**.

[**0255**] Not shown in **FIG. 20A** is a headband system comprised of two or more pads **880**A, **880**B, as shown in FIGS. **20**B-**20**E.

[**0256**] To allow for the broadest range of head sizes, the headband frame **861** utilizes two contoured foam pads **880**A and **880**B, angled, and spaced apart such that both small and large forehead curvature are accommodated. Each foam pad also has two primary contact areas **881** and **883**, that act in the same way. When combined with a strap **862** placed below the ball formed at the rear of the head, the net effect is that the headband frame **861** is securely located on the wearer's forehead **887** whether child or adult.

[**0257**] When the electronics are used, there is some heat being generated in the main housing or console **870**. Prior art headbands used wide forehead pads which effectively trapped this heat at the wearer's brow. This proved to be quite uncomfortable after extended wear.

[**0258**] The foam pads **880**A and **880**B displace the headband frame **861** from the user's forehead **887** leaving a gap