[0053] **FIG. 16A** is a plan view of an active matrix type display device according to the second embodiment;

[0054] **FIG. 16B** is a sectional view taken along a line **16**B-**16**B in **FIG. 16A**;

[0055] **FIG. 17A** is a plan view of an active matrix type display device according to the third embodiment;

[0056] **FIG. 17B** is a sectional view taken along a line **17**B-**17**B in **FIG. 17A**;

[0057] **FIG. 18** is a sectional view of an active matrix type display device according to the fourth embodiment;

[0058] **FIG. 19** is a sectional view of an active matrix type display device according to the fifth embodiment;

[0059] **FIG. 20A** is a plan view of an active matrix type display device according to the sixth embodiment;

[0060] **FIG. 20B** is a sectional view taken along a line **20**B-**20**B in **FIG. 20A**;

[0061] FIGS. **21** to **23** are sectional views showing the manufacturing steps of the active matrix type display device according to the sixth embodiment step by step;

[0062] **FIGS. 24A** to **29**B are views showing the manufacturing steps of the active matrix type display device according to the sixth embodiment step by step, in which views having suffix A are plan views, and views having suffix B are sectional views taken along lines designated by numbers suffixed with B in the corresponding plan views;

[0063] **FIG. 30A** is a plan view of an active matrix type display device according to the seventh embodiment;

[0064] **FIG. 30B** is a sectional view taken along a line **30**B-**30**B in **FIG. 30A**;

[0065] **FIG. 31A** is a plan view of an active matrix type display device according to the eighth embodiment;

[0066] **FIG. 31B** is a sectional view taken along a line **31**B-**31**B in **FIG. 31A**;

[0067] **FIG. 32A** is a plan view of an active matrix type display device according to the ninth embodiment;

[0068] **FIG. 32B** is a sectional view taken along a line **32**B-**32**B in **FIG. 32A**;

[0069] **FIG. 33** is a sectional view of an active matrix type display device according to the 10th embodiment;

[0070] **FIG. 34** is a sectional view of an active matrix type display device according to the 11th embodiment;

[0071] **FIG. 35** is a sectional view of an active matrix type display device according to a modification of the **11**th embodiment;

[0072] **FIG. 36** is a sectional view of an active matrix type display device according to another modification of the 11th embodiment;

[0073] **FIG. 37A** is a plan view showing the element arrangement of an active matrix type display device according to the 12th embodiment; and

[0074] **FIG. 37B** is a sectional view taken along a line **37**B-**37**B in **FIG. 37A**.

DETAILED DESCRIPTION OF THE INVENTION

[0075] Embodiments will be described in detail below with reference to the accompanying drawings.

[0076] (First Embodiment)

[0077] The arrangement of an active matrix type display device of the first embodiment is shown in **FIGS. 14A and 14B**. As indicated by a large rectangle of a dotted-line in **FIG. 14A, a** region on a substrate is divided into a pixel region and peripheral region. In the pixel region, active elements such as TFTs and pixel electrodes connected to these elements are formed into an array (not shown). In the peripheral region, a connecting pad electrode for connecting interconnections inside the substrate and interconnections extracted to the outside of the substrate is formed. Regions which are indicated by small rectangles of a dotted-line and in which a scanning line driver and signal line driver are formed are included in the pixel region in this embodiment. However, these regions may be formed in the peripheral region. In **FIG. 14**A, these drivers are formed in the peripheral region.

[0078] As shown in **FIGS. 2A and 2B**, the active matrix type display device of this embodiment includes a first plastic substrate **104**, a first adhesion layer **103** formed on the first plastic substrate **104**, and a first thin glass layer **101** having a thickness of 150 μm or less and formed on the first adhesion layer **103**.

[0079] The first adhesion layer **103** has a pixel region adhesion layer **1002** formed in the pixel region and a peripheral region adhesion layer **1001** formed in the peripheral region around the pixel region on the first plastic substrate **104**. The glass transition temperature of the pixel region adhesion layer **1002** is 30° C. (inclusive) to 80° C. (inclusive). The glass transition temperature of the peripheral region adhesion layer **1001** is higher by 10° C. or more than that of the pixel region adhesion layer **1002**, and is 80° C. (inclusive) to 200° C. (inclusive)

[0080] On the first thin glass layer **101**, an active element circuit region **102**, a connecting pad electrode **110** connected to the active element circuit region **102**, and a liquid crystal layer **109** (display part) are formed. This liquid crystal layer **109** is driven by the active element circuit region **102** in units of pixels. The connecting pad electrode **110** is formed on the peripheral region of the first glass layer **101**.

[0081] Also, a second thin glass layer **105** is formed over the liquid crystal layer **109**, a second adhesion layer **106** is formed on the second thin glass layer **105**, and a second plastic substrate **107** is formed on the second adhesion layer **106**. A common electrode **205** is formed on that surface of the second thin glass layer **105**, which opposes the liquid crystal layer **109**.

[0082] The thickness of the second thin glass layer **105** is 150 μm or less. The second adhesion layer **106** has a pixel region adhesion layer **1002** and peripheral region adhesion layer **1001**. The pixel region adhesion layer **1002** is formed in the pixel region and has a glass transition temperature of 30° C. (inclusive) to 80° C. (inclusive). The peripheral region adhesion layer **1001** is formed in the peripheral region around the pixel region on the second thin glass layer **105**, and has a glass transition temperature which is higher