

devices. Also, when a reflecting plate is placed in the liquid crystal cell to use this display device as a reflecting type display device, the polarizer/retardation film **206** can be formed only on the second plastic substrate **107**. The polarizer can also be omitted if the liquid crystal is in a scattering, interference display mode.

[0110] In this embodiment, the liquid crystal is injected after the cell is formed by bonding the plastic substrates to the thin glass layers. However, the following assembling method is also usable.

[0111] First, first and second non-alkaline glass substrates are thinned to form first and second thin glass layers, respectively. After first and second plastic substrates are bonded to these thin glass layers, a sealing portion made of an ultraviolet ray curable adhesive is formed on one glass substrate. A liquid crystal is injected inside this sealing portion, and the sealing portion is covered with the other glass substrate and hardened to bond the two glass substrates. In this method, the injection hole **204** is not formed. FIG. 2A shows this arrangement having no injection hole. Otherwise, when two thick glass substrates are bonded as shown in FIG. 5, liquid crystal may be dropped onto the display portion, and then the two glass substrates are sealed. After the sealing, the two glass substrates are polished to thin, followed by attaching the plastic substrates.

[0112] An example of the structure of an element usable in the active matrix type display device of this embodiment will be described with reference to FIGS. 14A and 14B. Although the display device has only two pixels in FIGS. 14A and 14B, a large number of pixels are actually formed in a matrix manner when viewed from the display surface.

[0113] Of the structure shown in FIGS. 14A and 14B, a portion different from FIGS. 2A and 2B, i.e., a portion from the first thin glass layer **101** to the second thin glass layer **105** will be explained.

[0114] On the first thin glass layer **101**, first and second undercoat insulating films **315** and **316** are stacked, and a polysilicon film including an active layer **302** and source/drain regions **303** is formed in each pixel. A gate insulating film **304** is formed on the entire surface. On this gate insulating film **304**, gate electrodes **305** are formed in regions corresponding to the active layers **302**. On top of these gate electrodes **305**, an interlayer dielectric film **306** is formed on the entire surface. On this interlayer dielectric film **306**, source electrodes **307** and drain electrodes **308** connecting to the source/drain regions **303** via contact holes are formed.

[0115] Interconnections such as scanning/signal lines **320** are formed in the same layer as the source electrodes **307** and drain electrodes **308**. Covering these interconnections, a passivation film **321** is formed on the entire surface. On this passivation film **321**, color filter layers **309** are formed in regions corresponding to the individual pixels. On these color filter layers **309**, pixel electrodes **310** connecting to the drain electrodes **308** via contact holes are formed. The pixel region in which these components are formed is surrounded by the seal **108**, and the second thin glass layer **105** is placed on it. The common electrode **205** is formed on that surface of this second thin glass layer **105**, which opposes the pixel region. In the space surrounded by the pixel region, common electrode **205**, and seal **108**, a liquid crystal is injected to form the liquid crystal layer **109**.

[0116] In a region not participating in display, pillars **311** are formed every few pixels between the color filter layers **309** and common electrode **205**. When external stress such as bending is applied, these pillars **311** absorb the force. Although fiber-like pillars or pearl-like pillars can be used, the pillars **311** are not limited to these forms.

[0117] In the peripheral region around the pixel region, electrodes **312** are formed in the same layer as the interconnections such as the scanning/signal lines **320**, and connected to the common electrode **205** via transfer conductors **313**. These transfer conductors **313** are covered with resin protectors **314**. Likewise, an anisotropic conductive sheet **319** is formed on the connecting pad electrode **110** which is formed in the same layer as the interconnections such as the scanning/signal lines **320** in the peripheral region. Interconnections **318** formed on the surface of a flexible substrate **317** are connected via this anisotropic conductive sheet **319**.

[0118] A method of manufacturing the element having the structure as described above will be explained below. First, first and second undercoat insulating films **315** and **316** are formed on a first non-alkaline glass substrate **201**. The first undercoat insulating film **315** is formed to have a thickness of about 500 nm by using a silicon nitride film. The second undercoat insulating film **316** is formed to have a thickness of about 100 nm by using a silicon oxide film. These undercoat insulating films can be a single layer, or other materials are also usable. The film thickness is preferably about 100 to 500 nm.

[0119] On the second undercoat insulating film **316**, an amorphous silicon film which functions as active layers **302** and source/drain regions **303** is formed and patterned as a polysilicon layer after being crystallized by excimer laser annealing. Instead of simple laser emission, it is possible to use a technique by which an intensity profile is formed in laser emission to cause lateral crystal growth and increase the grain size, or a method which causes crystallization by heat without using any laser. In this heat crystallization, crystallization may be performed by using a metal such as Ni. The crystal grain size can be relatively small, e.g., about 0.1 μm to 10 μm , or as large as a single crystal. The grain boundary may be liked like a lattice. The source/drain regions **303** are formed by introducing n- and p-type impurities by ion implantation or mass-separated ion injection. After gate electrodes (to be described later) are formed, it is possible to apply a self-aligned structure using these gate electrodes as masks or apply an LDD (Lightly Doped Drain) structure in which a low-concentration doping region is sandwiched between each of the source/drain region **303** containing a high-concentration impurity and active layer **302**.

[0120] Subsequently, a silicon oxide film is formed as a gate insulating film **304** on the entire surface by plasma CVD or the like. Furthermore, gate electrodes **305** are formed in the regions corresponding to the active layers **302** by using, e.g., a metal or alloy such as Mo, MoW, MoTa, Al, or Al—Cu, or highly doped silicon.

[0121] On these gate electrodes **305**, an interlayer dielectric film **306** about 300 nm to 1 μm thick is formed using a silicon oxide film or the like. As this interlayer dielectric film **306**, an organic resin such as polyimide can be used.

[0122] Source electrodes **307** and drain electrodes **308** connecting to the source/drain regions **302** via through-holes