nium-carbon base region **320** of base/emitter structure **410** then flow over to polysilicon germanium-carbon base region **322** to be collected by metal base contact **326** of base/emitter structure **410**.

[0050] In addition, the flow of holes increases the potential of p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **410** in the region that lies adjacent to n+ region **332**, thereby forward biasing the junction between p-type single-crystal-silicon germanium-carbon base region **320** and n+ emitter region **332** of base/emitter structure **410**.

[0051] As a result, p-type single-crystal-silicon germanium-carbon base region **320** also injects holes into n+ emitter region **332**, and n+ emitter region **332** injects electrons into p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **410**. Some of the electrons injected into base region **320** drift over and are then swept into n-type collector region **314** across the broken down junction. The electrons swept into n-type collector region **314** are injected into p-well **510** across the forward-biased junction.

[0052] The SiGe DIAC ESD protection structures **400**, **500**, and **600** can be formed with only minor modifications to any conventional SiGe HBT process flow. FIGS. **7-21** show a series of cross-sectional views that illustrate an example of a method of forming the SiGe DIAC ESD protection structures **400**, **500**, and **600** in accordance with the present invention.

[0053] As shown in FIG. **7**, the method utilizes a conventionally-formed semiconductor structure **708** that includes a p− substrate **710**, and an n+ buried layer **712** that touches and lies over p− substrate **710**. In addition, semiconductor structure **708** includes an n-type collector region **714** that extends down from the top surface of semiconductor structure **708** to touch the top surface of n+ buried layer **712**, and a number of shallow trench isolation regions **718** that extend down from the top surface of semiconductor structure **708**.

[0054] As further shown in FIG. **7**, the method begins by epitaxially growing a p-type silicon germanium carbon layer **720** on semiconductor structure **708**. The regions above n-type collector region **714** grow as a single crystal silicon germanium carbon layer **722**, while the regions above the shallow trench isolation regions **718** grow as a polysilicon germanium carbon layer **724**. While silicon germanium carbon is illustrated in this example, other semiconductor materials can alternately be used.

[0055] As shown in FIG. **8**, after silicon germanium carbon layer **720** has been grown, a mask **726** is formed and patterned on silicon germanium carbon layer **720**. Following this, a p-type dopant, such as boron, is implanted to form p+ regions **730** in n-type collector region **714**, and p+ regions **732** in silicon germanium carbon layer **720**. Alternately, as shown in FIG. **9**, mask **726** can be patterned such that no p+ region **730** is formed, and the p+ regions **732** are formed in polysilicon germanium carbon layer **724**. Following the implant, mask **726** is removed.

[0056] Once mask **726** has been removed, as shown in FIG. **10**, a layer of isolation material **734**, such as a layer of oxide and an overlying layer of nitride, is formed on silicon germanium carbon layer **720**. Next, a mask **736** is formed and patterned on isolation layer **734**. Following this, the exposed regions of isolation layer **734** are etched away. Mask **736** is then removed.

[0057] As shown in FIG. **11**, the etch forms an isolation region **740** and an isolation region **742**. Next, as shown in FIG. **12**, a layer of n+ polysilicon **744** is formed on silicon germanium carbon layer **720** and the isolation regions **740** and **742**. After polysilicon layer **744** has been formed, a mask **746** is formed and patterned on polysilicon layer **744**. Following this, as shown in FIG. **13**, the exposed regions of polysilicon layer **744** are etched away to form an emitter region **750** that touches isolation region **740** and silicon germanium carbon layer **720**, and an emitter region **752** that touches isolation region **742** and silicon germanium carbon layer **720**. In addition, both emitter regions **750** and **752** lie over a common isolation region **718**C. Following the etch, mask **746** is removed.

[0058] As shown in FIG. **14**, after the formation of the emitter regions **750** and **752**, a layer of silicide **754** is formed on the exposed regions of silicon germanium carbon layer **720** and the emitter regions **750** and **752**. Following this, a mask **756** is formed and patterned on the isolation regions **740** and **742**, and silicide layer **754**.

[0059] Next, as shown in FIG. **15**, the exposed regions of silicide layer **754** and the underlying regions of silicon germanium carbon layer **720** are etched away. The etch forms a base/emitter structure **760** and a base/emitter structure **762** that both touch common isolation region **718**C. Mask **756** is then removed.

[0060] Once mask **756** has been removed, as shown in FIG. **16**, a layer is insulation material **764** is formed on the exposed regions of the isolation regions **718**, silicon germanium carbon layer **720**, and the base/emitter structures **760** and **762**. Next, a mask **766** is formed and patterned on insulation layer **764**. Following this, the exposed regions of insulation layer **764** are etched to form openings **770** that expose the silicide layers **754**. Mask **766** is then removed.

[0061] Next, as shown in FIG. **17**, a layer of conductive material **772** is deposited on insulation layer **764** to fill up the openings **770**. Following this, a mask **774** is formed and patterned on conductive layer **772**. After mask **774** has been formed, the exposed regions of conductive layer **772** are etched until removed. Mask **774** is then removed.

[0062] As shown in FIG. **18**, the etch forms a first contact **780**, a second contact **782**, a first metal trace **784** that touches the first and second contacts **780** and **782**. The etch also forms a third contact **790**, a fourth contact **792**, and a second metal trace **794** that touches the third and fourth contacts **790** and **792**. First metal trace **784** electrically connects the polysilicon germanium carbon layer **720** of base/emitter structure **760** to the emitter region **750** of base/emitter structure **760**. Second metal trace **794** electrically connects the polysilicon germanium carbon layer **720** of base/emitter structure **762** to the emitter region **752** of base/emitter structure **762**.

[0063] The method then continues with conventional steps to form metal interconnect structures that include pads **796** and **798** that are connected to metal traces **784** and **794**, respectively. The described method is similar to the process for forming a SiGe HBT as taught in U.S. Pat. No. 7,202,136 issued on Apr. 10, 2007, which is hereby incorporated by reference.

[0064] SiGe DIAC ESD protection structure **500** can be formed in the same manner that structure **400** was formed, except that before silicon germanium carbon layer **720** is grown, a mask **1410** is formed on semiconductor structure **708** as shown in FIG. **19**. Following this, the exposed regions of semiconductor structure **708** are implanted with a p-type material, such as boron, to form a p-well **1412** that extends down and touches p− substrate **710**. Mask **1410** is then