

example, MoW are sequentially stacked on the undercoat layer UC to form top gate-type thin-film transistors. In this embodiment, the thin-film transistors are p-channel thin-film transistors and n-channel thin-film transistors. The p-channel thin-film transistors are utilized as drive control elements DR, switches SWa to SWc, and diodes D1a shown in **FIGS. 1 and 3**. The n-channel thin-film transistors are utilized as diodes D1b shown in **FIGS. 1 and 3**.

[0020] Bottom electrodes of capacitors C and scan signal lines SL1 and SL2 shown in **FIGS. 1 and 3** are further arranged on the gate insulator GI. These components can be formed in the same step as that for the gates G.

[0021] As shown in **FIG. 1**, the scan signal lines SL1 and SL2 extend along the rows of the pixels PX, i.e., in an X direction, and are arranged in a Y direction along the columns of the pixels PX. The scan signal lines SL1 and SL2 are connected to the scan signal line driver YDR.

[0022] An interlayer insulating film II shown in **FIG. 2** covers the gate insulator GI, the gates G, the scan signal lines SL1 and SL2, and the bottom electrodes of the capacitors C. The interlayer insulating film II is, for example, an SiO_x layer formed by plasma CVD. Parts of the interlayer insulating film II are utilized as dielectric layers of the capacitors C.

[0023] On the interlayer insulating film II, top electrodes of the capacitors C shown in **FIGS. 1 and 3**, source electrodes SE and drain electrodes DE shown in **FIG. 2**, and video signal lines DL and power supply lines PSL shown in **FIGS. 1 and 3** are arranged. These components can be formed in the same step and may have a three-layer structure of, for example, Mo, Al, and Mo.

[0024] The source electrodes SE and drain electrodes DE are electrically connected to sources and drains of the thin-film transistors via contact holes formed in the interlayer insulating film II.

[0025] As shown in **FIG. 1**, the video signal lines DL extend in the Y direction and are arranged in the X direction. The video signal lines DL are connected to the video signal line driver XDR.

[0026] The power supply lines PSL extend in the Y direction and are arranged in the X direction, for example.

[0027] A passivation film PS shown in **FIG. 2** covers the source electrodes SE, drain electrodes DE, video signal lines DL, power supply lines PSL, and top electrodes of the capacitors C. The passivation film PS is made of, for example, SiN_x.

[0028] As shown in **FIG. 2**, light-transmissive first electrodes PE as front electrodes are arranged on the passivation film PS such that they are spaced apart from one another. Each of the first electrodes PE is a pixel electrode connected through a through-hole formed in the passivation film PS to the drain electrode DE to which the drain of the switch SWa is connected.

[0029] In this embodiment, the first electrode PE is an anode. A transparent conductive oxide, for example, indium tin oxide (ITO) can be used as a material of the first electrode PE.

[0030] A partition insulating layer PI shown in **FIG. 2** is further placed on the passivation film PS. The partition

insulating layer PI has through-holes formed at positions corresponding to the first electrodes PE or slits formed at positions corresponding to columns or rows formed by the first electrodes PE. Here, by way of example, the partition insulating layer PI has through-holes formed at positions corresponding to the first electrodes PE.

[0031] The partition insulating layer PI is, for example, an organic insulating layer. The partition insulating layer PI can be formed using, for example, a photolithography technique.

[0032] An organic layer ORG including an emitting layer is placed on each of the first electrodes PE as an active layer. The emitting layer is, for example, a thin film containing a luminescent organic compound that emits red, green, or blue light. In addition to the emitting layer, the organic layer ORG may include a hole injection layer, a hole transporting layer, a hole blocking layer, an electron transporting layer, and an electron injection layer.

[0033] The partition insulating layer PI and the organic layer ORG are covered with a second electrode CE as a counter electrode. The second electrode CE is a common electrode shared among the pixels PX. In this embodiment, the second electrode CE is a light-reflective cathode serving as a back electrode. For example, an electrode wire (not shown) is formed on the layer on which the video signal lines DL are formed, and the second electrode CE is electrically connected to the electrode wire via a contact hole formed in the passivation film PS and partition insulating layer PI. Each organic EL element OLED is composed of the first electrode PE, organic layer ORG, and second electrode CE.

[0034] A plurality of the pixels PX are arranged in a matrix on the insulating substrate SUB. Each of the pixels PX is placed near an intersection of the video signal line DL and scan signal line SL1.

[0035] Each pixel PX includes the organic EL element OLED as a display element, a drive circuit, and an output control switch SWa. In this embodiment, as shown in **FIGS. 1 and 3**, the drive circuit includes a drive control element DR, a selector switch SWb, a diode-connecting switch SWc, and the capacitor C. As described above, in this embodiment, the drive control element DR and switches SWa to SWc are p-channel thin-film transistors. The switches SWb and SWc form a switch group which switches between a first state that the drain and gate of the drive control element DR and the video signal line DL are connected to one another and a second state they are disconnected from one another.

[0036] The drive control element DR, the output control switch SWa, and the organic EL element OLED are connected in series between a first power supply terminal ND1 and a second power supply terminal ND2 in this order. In this embodiment, the first power supply terminal ND1 is a high-potential power supply terminal connected to a power supply line PSL. The second power supply terminal ND2 is a low-potential power supply terminal.

[0037] A gate of the switch SWa is connected to the scan signal line SL1. The selector switch SWb is connected between the video signal line DL and the drain of the drive control element DR. The gate of the selector switch SWb is connected to the scan signal line SL2. The diode-connecting switch SWc is connected between the drain and gate of the