

DETAILED DESCRIPTION

[0020] Several embodiments of the invention with reference to the appended drawings are now explained. Whenever the shapes, relative positions and other aspects of the parts described below are not clearly defined, the scope of the invention is not limited only to the parts shown, which are meant merely for the purpose of illustration. Also, while numerous details are set forth, it is understood that some embodiments of the invention may be practiced without these details. In other instances, well-known circuits, structures, and techniques have not been shown in detail so as not to obscure the understanding of this description.

[0021] FIG. 1 depicts a reconfigurable PV system 1 in accordance with an embodiment of the invention. The system is composed of a number of PV energy harvesting sub-arrays 2. Although only four are shown, the system is of course not limited to that number as there may be as few as two sub-arrays 2 or there can be greater than four. Each sub-array 2 contains a group of PV cells 3 that are electrically connected to each other in series for a desired higher output voltage (see FIG. 4), in parallel for a desired increased current, or in a series-parallel combination to yield both higher output voltage and higher current (see FIG. 5). Mixed or non-symmetrical arrangements of parallel connected series strings of cells are also possible. The cell 3 may be a microsystem enabled photovoltaic (MEPV) cell that can be manufactured using semiconductor microelectronic fabrication techniques and be may relatively small, e.g., between 100 microns and 5 mm in diameter, and as low as 1 micron in thickness such as in a III-V semiconductor cell. Given the small size of the MEPV cell, the sub-array 2 can have thousands of cells 3 (in contrast to the 72 cells in a conventional PV module). Note also that not all of the cells 3 in a sub-array 2 need be replicates or even of the same type. For example, some may be silicon others may be Ge or III-V cells. The cell 3 may alternatively be a multi-junction cell that has a combination of two or more junctions that may be connected in series or, as described below in accordance with an embodiment of the invention depicted in FIGS. 7-8. For example, each of the sub-arrays 2 may be composed of photocells each of which has an active or light detection area that is less than five (5) square millimeters in area, and wherein each of the sub-arrays 2 may have several thousand of MEPV photocells and may produce between 1 volt (e.g., two Si silicon cells in series) and 1000 volts dc, with currents in the range 1 uAmpere to several Amperes, uAmperes for applications where only high voltage and low or essentially no current is needed (electron/ion acceleration grids, for example), and several Amperes for high current draw applications (e.g., thermal loads, etc.) it would be possible to transfer mW to kW of power using the power transfer configuration described here.

[0022] Still referring to FIG. 1, in the presence of incident light, a sub-array output voltage is produced by each sub-array 2, from its connected cells 3, at a respective pair of sub-array power nodes. These are sometimes designated with the labels (+) and (-) to indicate the polarity of the output voltage. The output voltage and current or output power of the sub-array is delivered by a distributed network of conductors and active circuits referred to here as a power grid. The power grid (or power bus interconnect) is composed of multiple bus rows and multiple bus columns. As can be seen, a bus management circuit 5 is positioned at a respective junction of a bus column and a bus row. Each bus row has a respective number of bus group row segments 6 that are coupled in a

daisy chain manner, or forming a sequence, by some of the bus management circuits 5. Similarly, each bus column has a respective number of bus group column segments 7 that are also coupled in a daisy chain manner, by some of the bus management circuits 5. Each bus group segment (row segment 6 or column segment 7) has a respective number of bus conductors. In one example, each bus group segment has two bus conductors, as seen in FIG. 2 and in FIG. 3, although additional conductors may be added in parallel, for example, to reduce electrical resistance. In such a power grid, each bus management circuit 5 may be coupled to between two and four adjacent bus group segments, namely left and right bus group row segments 6, and upper and lower bus group columns segments 7.

[0023] Coupled to each pair of sub-array output power nodes is the input of a respective sub-array power management circuit 4. The circuit 4 also has a power output that is coupled to the power grid, i.e., to either a row segment 6 or a column segment 7. In one embodiment, the current path switches in each sub-array power management circuit 4 support a "mesh network" in that they can connect any of the input nodes of the circuit 4 with any of its output nodes. The circuit 4 also has a communications interface, which is not shown in FIG. 1 but can be seen in FIG. 2 where it is coupled to a communications grid 9. The communications grid 9 to which the communications interfaces of the power management circuits 4 and bus management circuits 5 are coupled may be any suitable, relative low complexity and low bit rate digital communications bus. This communication interface could be optical in nature with the information passed to the power management circuit through a signal encoded on the light that is illuminating the sub-arrays and that is decoded by a communications band decoder—see FIG. 2 described below.

[0024] The sub-array power management circuit 4 contains circuitry including solid state current path switches, switch drivers, control logic, and communications interface circuitry that enables it to be programmable (through its communication interface) during in-the-field use of the PV system, to either connect or disconnect its respective sub-array 2 to the power grid. In addition to the programmable sub-array power management circuits 4, each of the bus management circuits 5 is also programmable (through its communication interface) to one of connect and disconnect a power or current path in the power grid, using internal current path switches that may also support a mesh network (similar to the capability of the circuit 4 described above). Those two capabilities together enable two or more selected sub-arrays 2 to be connected, through selected current or power paths in a "programmable" power grid, in parallel so as to produce a low voltage at the harvested energy output node but at a high current. Alternately, the configurability of the sub-array power management circuits 4 and the bus management circuits 5 enable two or more selected sub-arrays 2 to be connected, via selected current paths, in series so as to produce a higher voltage that may be greater than the lower voltage by at least a factor of ten (depending upon a sufficient number of sub-arrays 2 being available for a series connection).

[0025] Referring now to FIG. 2 for additional details concerning the power grid and the sub-array power management circuits 4, FIG. 2 shows an example power path that has been created in the power grid, by appropriately programming the current path switches in selected circuits 4, 5. The example power path enables a series connection of sub-arrays 2_1,