

-continued

Power Down Control
 ARC processor core
 Internal control registers
 Interrupt Controller
 Timers
 WEP engine
 DMA Controllers

[0026] The lower MAC 150 is designed to interface with the baseband processor on the one hand and the upper MAC 210 on the other. Specifically, the interface must be able to keep up with the data flow from the baseband processor, both for transmit and receive. Such a data flow may currently be as fast as 11 megabits per second and is expected to be as high as 100 megabits per, second in the near future. The enabling of WEP (for encrypting and decrypting) may be activated so as not to adversely affect throughput.

[0027] With respect to the interface with the upper MAC 210, the lower MAC 150 is designed so that its implementation does not vary based on whatever device will ultimately receive the signals sent via the RF medium. In order for such an interface to work properly, certain information regarding the nature of the host device 240 (and the upper MAC 210, which is host device 240 dependent) must be incorporated into the process of the lower MAC 150. Such incorporation may occur, for example, by software or hardware.

[0028] In particular, various types of information may be stored in registered included in the lower MAC 150 to accomplish the necessary interface with the upper MAC 210. To provide for the possibility that problems that can occur when the host device 240 is operating, the lower MAC 150 may operate completely asynchronously to the interface with the upper MAC 210 by providing all of the registers with double synchronizing flip flops on all the communication signals and data latches. The interface may be designed to work with processors that have bus speeds of up to 100Mhz while being completely static for very slow access requirements.

[0029] In a further example, the lower MAC 150 may include one or more hardware configuration registers to represent the bus size of the host device 240. In one embodiment, the size of the bus of the host, which may be, for example, an 8, 16, or 32 bit bus is softloaded into a register located in the lower MAC 150. This may be accomplished via software (preferred embodiment) or via hardware using external pins. The register may consist of two double synchronizing flip flops that can be set to indicate the width of the bus of the host device 240 in accordance with the following table:

00-Not Valid
01-8 bits
10-16 bits
11-32 bits

[0030] In a further embodiment, this hardware configuration register may be configured prior to setting a "System

Enable" control bit and it is never modified while the system is enabled. Because setting this register involves a test modes that have special functions and require an intimate knowledge of the internal logic to use them effectively, they are not be used during normal operation. Accordingly, this register may be written twice with the same data value in order for the configuration to take effect.

[0031] In a further embodiment, the functionality of the hardware configuration registers may be accomplished instead by software running within the lower MAC 150.

[0032] These configurations may be set to work with optional features of the MAC layer in the 802.11 protocol. One MAC-layer problem specific to wireless is the "hidden node" issue, in which two stations on opposite sides of an access point can both "hear" activity from an access point, but not from each other, usually due to distance or an obstruction. To solve this problem, 802.11 specifies an optional Request to Send/Clear to Send (RTS/CTS) protocol at the MAC layer. When this feature is in use, a sending station transmits an RTS and waits for the access point to reply with a CTS. Since all stations in the network can hear the access point, the CTS causes them to delay any intended transmissions, allowing the sending station to transmit and receive a packet acknowledgment without any chance of collision. Since RTS/CTS adds additional overhead to the network by temporarily reserving the medium, it is typically used only on the largest-sized packets, for which retransmission would be expensive from a bandwidth standpoint.

[0033] The 802.11 MAC layer provides for two other robustness features: CRC checksum and packet fragmentation. Each packet has a CRC checksum calculated and attached to ensure that the data was not corrupted in transit. This is different from Ethernet, where higher-level protocols such as TCP handle error checking. Packet fragmentation allows large packets to be broken into smaller units when sent over the air, which is useful in very congested environments or when interference is a factor, since larger packets have a better chance of being corrupted. This technique reduces the need for retransmission in many cases and thus improves overall wireless network performance. The MAC layer is responsible for reassembling fragments received, rendering the process transparent to higher-level protocols.

[0034] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

I claim:

1. A system for processing radio frequency signals, comprising:
 - a transceiver for the reception and transmission of radio frequency signals;
 - a frequency converter for converting the radio frequency signals into an analog baseband signal, the analog baseband signal having a frequency less than the frequency of the radio frequency signal;
 - a baseband processor for converting the analog baseband signal into a corresponding digital signal;