

disclosed elsewhere herein in the Detailed Description, and particularly pointed out in the claims filed with the application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention may best be understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0013] FIG. 1 is a block flow diagram of an embodiment of a method of separating semiconductor devices from a substrate by etching a release layer.

[0014] FIGS. 2A-2C are cross-sectional side views of embodiments of workpiece objects at different stages of an embodiment of an approach for separating semiconductor devices from a substrate by etching a release layer.

[0015] FIGS. 3A-3I are cross-sectional side views of embodiments of workpiece objects at different stages of an embodiment of an approach for separating group III-V compound semiconductor devices from a substrate by etching a graded composition group III-V compound semiconductor release layer.

[0016] FIG. 4 is a cross-sectional side view of an embodiment of a workpiece object including a first embodiment of a suitable set of materials.

[0017] FIG. 5 is a cross-sectional side view of an embodiment of a workpiece object including a second embodiment of a suitable set of materials.

[0018] FIGS. 6A-6D are cross-sectional side views illustrating several other embodiments of suitable protuberances.

[0019] FIG. 7 is a block flow diagram of an embodiment of a method of separating semiconductor devices from a substrate using first and second receiving substrates.

[0020] FIG. 8 is a block flow diagram of an embodiment of a method of reusing a substrate.

DETAILED DESCRIPTION

[0021] In the following description, numerous specific details are set forth (e.g., specific types of semiconductor devices, device structures, materials, orders of operations, and the like). However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0022] FIG. 1 is a block flow diagram of an embodiment of a method 100 of separating semiconductor devices from a substrate by etching a release layer. FIGS. 2A-2C are cross-sectional side views of embodiments of workpiece objects (e.g., in-process wafers or other intermediate substrates) at different stages of an embodiment of a method of separating semiconductor devices from a substrate by etching a release layer. To facilitate the description, the method of FIG. 1 will be described in conjunction with the views of FIGS. 2A-2C. The components, features, and optional details described for the workpiece objects of FIGS. 2A-2C also optionally apply to the operations and/or method of FIG. 1, which in embodiments may be performed using such workpiece objects. However, it is to be appreciated that the operations and/or method of FIG. 1 may be used with different substrates than those of FIGS. 2A-2C. Moreover, the workpiece objects of FIGS. 2A-2C may be used with different operations and/or methods than those of FIG. 1.

[0023] Referring initially to FIG. 1, the method includes providing a workpiece object, at block 101. The workpiece object may represent an in-process wafer, other intermediate substrate, or other workpiece object used to form semiconductor devices during a manufacturing process. As used herein, “providing” the workpiece object is to be interpreted broadly as fabricating, purchasing, trading for, or otherwise obtaining the workpiece object. In some embodiments, the workpiece object may have a release layer that is coupled between multiple semiconductor devices and a substrate. In some embodiments, the release layer may be a graded composition release layer in which a concentration or other composition of at least one component is graded across a thickness of the graded composition release layer. Alternatively, a non-graded composition or homogeneous composition release layer may optionally be used.

[0024] Turning now to FIG. 2A, an embodiment of workpiece object 210A includes a substrate 212, a release layer 214, and semiconductor devices 216-1, 216-2 (collectively semiconductor devices 216). The substrate is to be interpreted broadly herein. In one example, the substrate may be a semiconductor substrate that includes a wafer or other piece of semiconductor material optionally having one or more semiconductor layers formed thereon. In another example, the substrate may include a support substrate (e.g., a silicon substrate, a ceramic substrate, a glass substrate, etc.) having one or more semiconductor layers formed thereon. It is to be appreciated that in some implementations the semiconductor substrate may also optionally include other materials besides just semiconductors, such as, for example, dielectric materials, metals, and other materials commonly found in the substrates on which semiconductor devices are formed.

[0025] The semiconductor devices 216 have been formed over the substrate 212. For simplicity, the illustration only shows a first semiconductor device 216-1 and a second semiconductor device 216-2, although it is to be appreciated that there may be any desired number of such semiconductor devices. For example, there may be a two-dimensional array of such devices, for example, including on the order of from tens to many thousands of such devices. For example, in one particular embodiment, the substrate may measure several inches in cross-section, each of the semiconductor devices may measure several millimeters or less (or in sonic cases 1 mm or less) in cross-section, and the semiconductor devices may be arranged in a two dimensional array fit substantially as many as possible over the substrate. In the case of photovoltaic cells, the ability to produce such small cells may offer various possible advantages, such as, for example, generally favorable photovoltaic efficiencies, various scaling effects due the size, an ability to make flexible solar panels, etc. However, it is to be appreciated that the scope of the invention is not limited to any known number of such semiconductor devices.

[0026] In sonic embodiments, the semiconductor devices 216 may include photovoltaic cells or other photovoltaic devices. Each photovoltaic cell or device may include either a single photovoltaic “pixel” or multiple photovoltaic “pixels”. In some cases, each photovoltaic cell or device may include a two-dimensional array having on the order of tens, to on the order of hundreds, of such photovoltaic pixels, although the scope of the invention is not so limited. In some embodiments, the photovoltaic cells or devices may represent group III-V compound semiconductor photovoltaic cells or devices, although the scope of the invention is not so limited. In other