

embodiments, other semiconductor devices besides photovoltaic devices may be used. Examples of other suitable types of semiconductor devices include, but are not limited to, photodiode arrays, semiconductor laser devices (e.g., vertical-cavity surface-emitting lasers (VCELs)), other group III-V compound semiconductor devices, other types of integrated circuits (e.g., microcontrollers, microelectromechanical systems (MEMS)), or the like.

[0027] The present disclosure refers to group III-V compound semiconductor devices. The term compound semiconductor generally refers to a semiconductor compound composed of elements from two or more different groups of the periodic table. The term group III-V compound semiconductor refers to an old/legacy naming convention which is still used today in the arts. It is to be appreciated that the group III-V compound semiconductors may alternatively be referred to as group 13-15 compound semiconductors using the present day nomenclature. Group 13 includes the elements boron (B), aluminum (Al), gallium (Ga), indium (In), and thallium (Tl), and is sometimes referred to as the boron group. Group 15 includes the elements nitrogen (N), phosphorus (P), arsenic (As), antimony (Sb), and bismuth (Bi), and is sometimes referred to as the nitrogen group or the pnictogens.

[0028] The release layer **214** is coupled between the semiconductor devices **216** and the substrate **212**. In the illustration, the semiconductor devices are formed over the release layer, and the release layer is formed over the substrate. The terms “coupled” and “connected,” along with their derivatives, may be used herein. These terms are not intended as synonyms for each other. Rather, in particular embodiments, “connected” may be used to indicate that two or more elements are in direct physical and/or electrical contact with each other. “Coupled” may mean that two or more elements are in direct physical or electrical contact with each other. However, “coupled” may also mean that two or more elements are not in direct contact with each other. For example, the release layer may be coupled with substrate and/or the semiconductor devices through one or more intervening elements (e.g., layers, materials, structures, etc.). Similarly, a first element “over” a second element may refer to either the first element directly “on” the second element, or there may be one or more intervening elements disposed between the first and second elements. Furthermore, it should be noted that terms such as “over,” “under,” “top,” “bottom,” “vertical,” “horizontal,” and the like, are used herein to refer to the structures as viewed in the illustrations, although the structures may be used in a variety of different orientations.

[0029] In some embodiments, as the name implies, the release layer may be etched to help release the semiconductor devices from the substrate. In some embodiments, the release layer may have a thickness ranging from about 200 Å to about 10 μm, or in some cases from about 500 Å to about 5 μm, although the scope of the invention is not so limited. In some embodiments, the release layer may be a graded composition release layer in which a concentration or other composition of at least one component may be graded across a thickness of the layer. The gradation in the composition of the at least one component may change gradually and continuously (e.g., linearly, nonlinearly, etc.), by a series of two or three or more discrete or stepwise levels, or a combination thereof. By way of example, in one embodiment suitable for group III-V compound semiconductor devices, the graded composition release layer may include a graded indium-gallium-arsenide

to indium-gallium-arsenide-phosphorous layer in which a relative composition of phosphorous to arsenic changes across a thickness of the layer, although the scope of the invention is not so limited. In some embodiments, the graded composition may modify an etch rate of a given etch.

[0030] Referring again to FIG. 1, the method includes etching the release layer with an etch, at block **102**. In some embodiments, the release layer may be a graded composition release layer and the etch may have an etch rate that depends on the composition of the at least one component that is graded across the thickness of the graded composition release layer, although the scope of the invention is not so limited. The change in the composition of the at least one component across the layer may change the etch rate. As a result, the etch rate may vary with depth across the thickness of the graded composition release layer. In some embodiments, the etching may include etching the release layer between the semiconductor devices and the substrate until the semiconductor devices are at least substantially released from the substrate. The etch may etch under the semiconductor devices (e.g., undercut the semiconductor devices). As used herein, the term “substantially released” encompasses either released and/or released enough that the semiconductor devices can be separated from the substrate using a given approach to couple a receiving substrate, as discussed further below.

[0031] In some embodiments, the etching at block **102** may include shaping, forming, carving, or otherwise etching a protuberance in the release layer (e.g., shaping the protuberance out of the release layer) between each of the semiconductor devices and the substrate. As used herein, the term “protuberance” refers broadly to a structure that bulges, protrudes, extends, or otherwise protrudes from a surface. Examples of suitable protuberances include, but are not limited to, structures, materials, surfaces, or other elements in the form of bulges (e.g., elements that bulge out from a surface), protrusions (e.g., elements that protrude from a surface), convexities (e.g., elements that are curved or rounded outwardly), humps, mounds, hills, hemispherical elements, conical shapes, truncated conical shapes, raised mesas, and the like, and combinations thereof. The protuberances provide a non-flat (i.e., non-coplanar, curved, rounded, etc.) surface between each of the semiconductor devices and the substrate. Accordingly, the etching may involve forming a non-flat (i.e., non-coplanar, curved, rounded, etc.) surface between each of the semiconductor devices and the substrate. The duration of the etch and the positions and sizes of the etch access openings may be used to control the shape of the protuberance. In addition, in embodiments that use a graded composition release layer, the variation in the etch rate with the variation in the graded composition may also be used to control the size and shape of the protuberances. In such cases, the protuberances formed from the the graded composition release layer may represent graded composition protuberances that have a graded composition across their thickness.

[0032] After the etching at block **102**, the method includes stopping the etch at block **103**. In some embodiments, the etch is stopped after the semiconductor devices have been at least substantially released, and while the protuberances and/or the non-flat surfaces remain between each of the semiconductor devices and the substrate. If the etch were allowed to continue further, the protuberances would be etched further and decrease in size and may generally would disappear entirely if the etch were allowed to proceed long enough.