

the top of the protuberance and/or non-flat surface. In such cases, a relatively weak coupling of the group III-V device with the protuberance may be broken or severed. Notice in the illustration that the protuberance remains behind still coupled with the substrate. In other embodiments, the protuberance may instead remain coupled with the group III-V device.

[0066] In some embodiments, the separation of the receiving substrate having the group III-V device coupled therewith from the substrate may be performed as part of a wafer-level lift off of multiple or potentially many such group III-V devices dispersed across the length of the substrate. In some embodiments, all such group III-V devices may be lifted off in one such lift-off operation with one receiving substrate. Alternatively, different groups or subsets of the group III-V devices may be lifted off during different lift-off operations with different receiving substrates. For example, two, three, or four, or more of such lift-off operations may be used. Advantageously, such ability to separate the group III-V devices from the substrate through the use of the receiving substrate may represent an efficient way to handle the group III-V devices and/or allow efficient assembly into a module, package, or other deployment. There may be no requirement to use a pick-and-place machine, or otherwise handle individual ones of the devices.

[0067] As previously mentioned, various different combinations of group III-V compound semiconductor and related materials may be used to form various different types of semiconductor devices. To further illustrate certain concepts, FIGS. 4-5 show several embodiments of suitable sets of materials, although the scope of the invention is not limited to just these materials.

[0068] FIG. 4 is a cross-sectional side view of an embodiment of a workpiece object **410** including a first embodiment of a suitable set of materials. The workpiece object includes a substrate **411**. As one example, the substrate may represent an indium phosphide (InP) substrate, although this is not required. An InP layer **412** is included in or formed over and/or on the substrate. A lattice matched graded composition indium-gallium-arsenide-phosphide (InGaAsP) to indium-gallium-arsenide (InGaAs) release layer **414** is formed over and/or on the InP layer **412**. In some embodiments, the composition of phosphorous may increase in the direction leading toward the InP layer **412** and/or from the top to the bottom of the layer (as viewed). An InP etch stop layer **499** is formed over the graded layer **414**. A lattice matched indium-gallium-arsenide (InGaAs) bottom contact layer **432** is formed over and/or on the graded composition release layer. A lattice matched set of group III-V compound semiconductor photovoltaic cell active layers **434** (or active layers for other types of group III-V compound semiconductor devices) are formed over and/or on the bottom contact layer. A lattice matched InGaAsP upper contact layer **436** is formed over and/or on the group III-V compound semiconductor active layers. Upper electrical contacts **438U** (e.g., gold pads) are formed over the InGaAsP upper contact layer.

[0069] FIG. 5 is a cross-sectional side view of an embodiment of a workpiece object **510** including a second embodiment of a suitable set of materials. The workpiece object includes a substrate **511**. As one example, the substrate may represent a gallium-arsenide (GaAs) substrate, although this is not required. A GaAs layer **512** is included or formed over and/or on the substrate **511**. A lattice matched graded composition indium-aluminum-phosphide (InAlP) to indium-aluminum-gallium-phosphide (InAlGaP) to indium-gallium-

phosphide (InGaP) release layer **514** is formed over and/or on the GaAs layer **512**. In some embodiments, the composition of gallium may increase in the direction leading toward the GaAs layer **512** and/or from the top to the bottom of the layer (as viewed). A lattice matched GaAs bottom contact layer **532** is formed over and/or on the graded composition release layer. A lattice matched set of group III-V compound semiconductor photovoltaic cell active layers **534** (or active layers for other types of group III-V compound semiconductor devices) are formed over and/or on the bottom contact layer. A lattice matched GaAs upper contact layer **536** is formed over and/or on the group III-V compound semiconductor active layers. Electrical contacts **538U** (e.g., gold pads) are formed over the AlGaAs upper contact layer.

[0070] It is to be appreciated that these are just a few illustrative examples of suitable materials. Other sets of suitable materials will be apparent to those skilled in the arts and having the benefit of the present disclosure. For example, sapphire materials, germanium based devices, gallium nitride based devices, or other materials known in the arts may be used.

[0071] FIGS. 6A-6D are cross-sectional side views illustrating several alternate embodiments of suitable protuberances **620**. Any of these protuberances may be used in any of the methods or approaches disclosed herein. In each of these embodiments, the protuberance **620** is disposed between a substrate **612** and a semiconductor device **616**.

[0072] FIG. 6A illustrates a first embodiment of a suitable protuberance **620A**. The protuberance has an approximately truncated conical shape with recessed or concave sidewalls. The semiconductor device is still partly directly connected to the protuberance at a relatively small area at the top of the protuberance (i.e., at the truncated part of the cone). The recessed or concave sidewalls may help to reduce the contact area between the semiconductor device with the protuberance in cases where the semiconductor device unintentionally slips or falls. Even if the semiconductor device were to slip or fall, it still would still generally contact the protuberance only at small surface areas due in part to the recessed or concave sidewalls. As discussed above, this may help to reduce stiction and/or other attractive forces.

[0073] FIG. 6B illustrates a second embodiment of a suitable protuberance **620B**. The protuberance has a central relatively flat mesa or top and recessed or concave sidewalls. The semiconductor device is fully released from the protuberance. Again in this embodiment, the recessed or concave sidewall may help to reduce the contact area between the semiconductor device with the protuberance in cases where the semiconductor device unintentionally slips or falls.

[0074] FIG. 6C illustrates a third embodiment of a suitable protuberance **620C**. The protuberance has a shape of a small bulge or mound or hill of material. The semiconductor device is fully released from the protuberance. Moreover, the protuberance has been further etched until it is relatively small. If the semiconductor device were to slip or fall, the protuberance may help to prevent the semiconductor device from lying flat on the top surface of the substrate. Rather, the semiconductor device will contact the protuberance at only a significantly smaller area should it fall. It should be appreciated that various otherwise shaped small protuberances (e.g., amounting to some sort of a bump, projection, or protuberance from the surface) may accomplish a similar objective of preventing the semiconductor device from lying flat on the top surface of the substrate should it slip or fall.