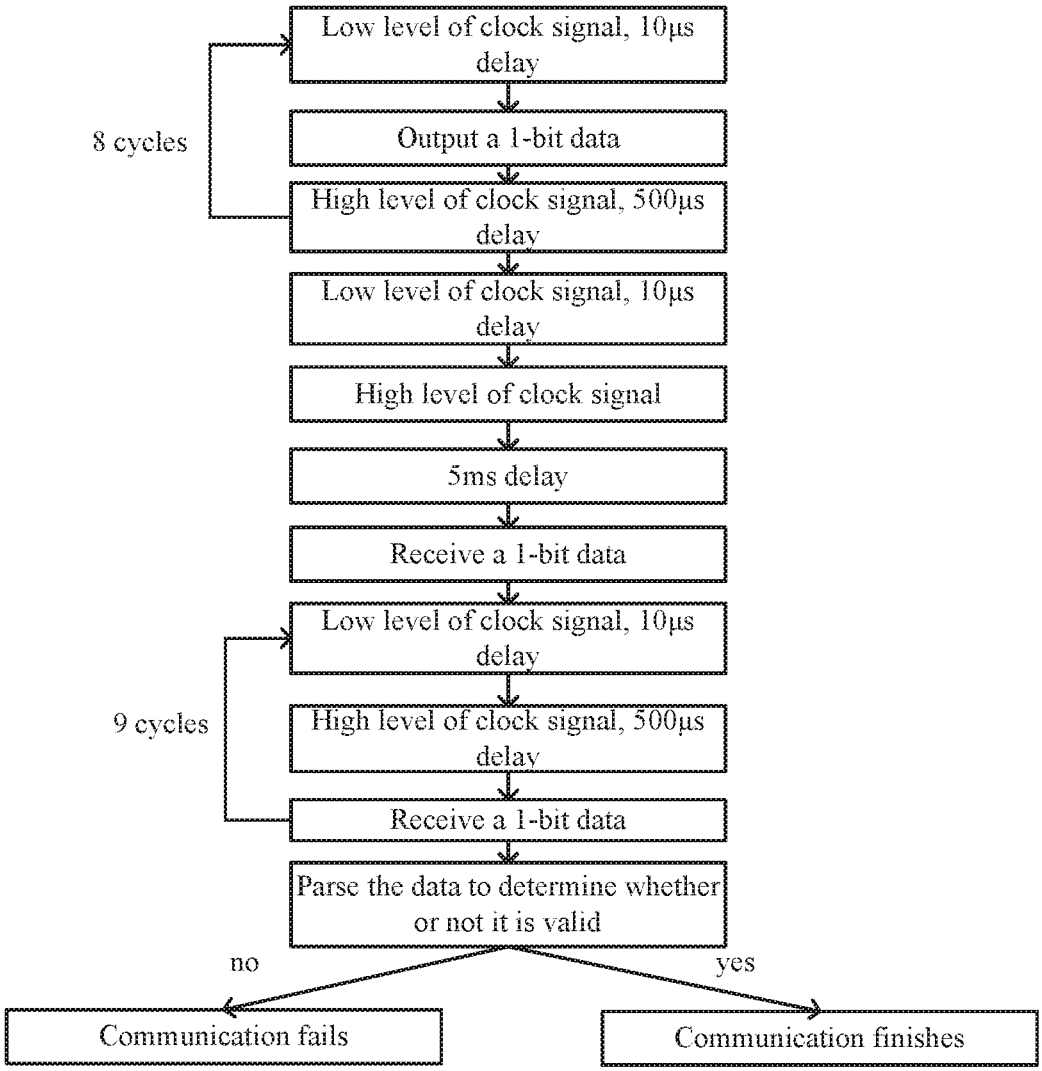
Low level of clock signal, 10μs delay
8 cycles
Output a 1-bit data
High level of clock signal, 500μs delay
Low level of clock signal, 10μs delay
High level of clock signal
5ms delay
Receive a 1-bit data
Low level of clock signal, 10μs delay
9 cycles
High level of clock signal, 500μs delay
Receive a 1-bit data
Parse the data to determine whether or not it is valid
no
yes
Communication fails
Communication finishes

FIG. 3

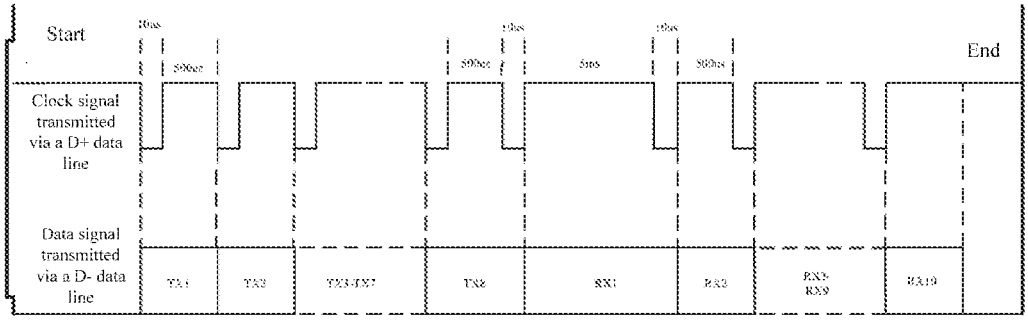
Start
End
Clock signal transmitted via a D+ data line
Data signal transmitted via a D- data line

FIG. 4