4. The transistor of claim **2**, wherein the second non-conducting spacer has a thickness of from about 500 Å to about 5000 Å.

5. The transistor of claim **1**, wherein the trench is further defined by the buffer layer, the transistor further comprising a thin GaN layer having a thickness of from about 2.0 to about 50.0 Å between the trench and the gate structure.

6. The transistor of claim **1**, wherein the gate structure comprises a dielectric layer and wherein the dielectric layer has a thickness of from about 60 Å to about 600 Å.

7. The transistor of claim **1**, wherein the trench is further defined by the buffer layer and wherein the gate structure comprises an aluminum nitride (AlN) layer on the spacer layer and in the trench and a dielectric layer on the AlN layer.

8. The transistor of claim **7**, wherein the AlN layer has a thickness of from about 1.0 Å to about 10.0 Å.

9. The transistor of claim **7**, wherein the AlN layer comprises an Aluminum Gallium Nitride (AlGaN) layer.

10. The transistor of claim **7**, further comprising a thin gallium nitride (GaN) layer having a thickness of from about 2.0 to about 50.0 Å between the AlN layer and the trench.

11. The transistor of claim **7**, wherein the gate structure further comprises a gallium nitride (GaN) layer on the AlN layer, the GaN layer being between the dielectric layer and the AlN layer.

12. The transistor of claim **11**, wherein the GaN layer has a thickness of from about 2.0 Å to about 30 Å.

13. The transistor of claim **11**, further comprising a thin gallium nitride (GaN) layer having a thickness of from about 2.0 to about 50.0 Å between the AlN layer and the trench.

14. The transistor of claim **1**, wherein the first non-conducting spacer comprises silicon nitride and has a thickness of from about 300 Å to about 3000 Å.

15. The transistor of claim **1**, wherein the gate electrode has a length of from about 0.5 μm to about 5.0 μm.

16. The transistor of claim **1**, wherein the transistor comprises a normally-off High Electron Mobility Transistor (HEMT).

17. A method of forming a semiconductor device, comprising:

forming a Group III-nitride buffer layer;

forming a Group III-nitride barrier layer on the Group III-nitride buffer layer;

forming a non-conducting spacer layer on the Group III-nitride barrier layer;

etching the Group III-nitride barrier layer and the spacer layer to form a trench, the trench extending through the barrier layer and exposing a portion of the buffer layer;

forming a gate structure on the spacer layer and in the trench; and

forming a gate electrode on the gate structure.

18. The method of claim **17**, wherein the forming the gate structure comprises forming a dielectric layer and wherein the dielectric layer has a thickness of from about 60 Å to about 600 Å.

19. The method of claim **17**, wherein etching further comprises etching a portion of the Group III-nitride buffer layer and wherein forming the gate structure comprises forming an aluminum nitride (AlN) layer on the spacer layer and in the trench and forming a dielectric layer on the AlN layer.

20. The method of claim **19**, wherein forming the gate structure further comprises forming a gallium nitride (GaN) layer on the AlN layer, the GaN layer being between the dielectric layer and the AlN layer.

21. A transistor, comprising:

a Group III-nitride barrier layer;

a non-conducting spacer layer on the Group III-nitride barrier layer, the spacer layer defining a trench extending through the spacer layer and exposing a portion of the barrier layer;

a gate implant region in a portion of the barrier layer; and

a gate electrode in the trench on the implanted region and on the spacer layer.

22. The transistor of claim **21**, further comprising dielectric sidewall spacers on a sidewall of the trench.

23. The transistor of claim **22**, wherein the implant region has an implant dose of from about 5.0×10^{12} cm^{-2} to about 1.0×10^{14} cm^{-2}.

24. The transistor of claim **22**, wherein the dielectric sidewall spacers have a thickness of from about 1.0 nm to about 50.0 nm.

25. The transistor of claim **21**, further comprising:

a second non-conducting spacer layer on the gate electrode and the spacer layer; and

a field plate on the second non-conducting spacer.

26. The transistor of claim **25**, wherein the field plate is electrically coupled to a source electrode or the gate electrode.

27. The transistor of claim **25**, wherein the second non-conducting spacer has a thickness of from about 500 Å to about 5000 Å.

28. The transistor of claim **21**, wherein the trench extends into the barrier layer.

29. The transistor of claim **28**, wherein the trench extends from about 0 Å to about 200 Å into the barrier layer.

30. The transistor of claim **21**, wherein the transistor comprises a normally-off High Electron Mobility Transistor (HEMT).

31. A method of fabricating a semiconductor device, comprising:

forming a Group III-nitride barrier layer;

forming a non-conducting spacer layer on the Group III-nitride barrier layer;

etching the spacer layer to form a trench, the trench extending through the spacer layer and exposing at least a portion of the Group III-nitride barrier layer;

forming a gate implant region in a portion of the barrier layer; and

forming a gate electrode in the trench on the gate implant region and on the spacer layer.

32. The method of claim **31**, wherein forming the gate implant region comprises:

implanting dopant ions into the exposed portion of the barrier layer with an implant energy of from about from about 3.0 keV to about 20 keV and a dose of from about 5.0×10^{12} cm^{-2} to about 1.0×10^{14} cm^{-2}; and

annealing the implanted dopant ions for from about 30 seconds to about 10 minutes at a temperature of from about 1000° C. to about 1300° C.

33. The method of claim **32**, wherein annealing the implanted dopant ions comprises annealing the implanted dopant ions in an ammonia containing atmosphere.

34. The method of claim **33**, wherein the dopant ions comprise magnesium (Mg) or zinc (Zn).

35. The method of claim **33**, wherein annealing the implanted dopant ions is followed by performing an activation anneal of the implanted dopant ions for about 1.0 minute to about 1.0 hour the implant at a temperature of from about 600° C. to about 900° C.

36. The method of claim **35**, wherein the activation anneal is performed in an atmosphere containing about 80 percent N_2 and 20 percent 0_2.

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