

Actuator operation

[0078] Integral to the design of the haptel in the preferred embodiment is actuator **504**. Actuator **504** is comprised of the following subset of haptel **500** parts: magnet **304**, flux disk **306**, midsection **316**, base **302**, magnet wire **108** and coil holder **104**. Magnet **304** creates and sustains a magnetic field, which is magnetically conducted upward through flux disk **306**, radially outwards across the air gap between the flux disk and midsection **316**, downward through the midsection, downward into base **302**, and radially inwards and upwards through the base, returning to the other side of the magnet. Thus a magnetic field of high flux density is created in the air gap between the flux disk and the midsection. This air gap is occupied by magnet wire **108** and coil holder **104**, which physically supports the magnet wire.

[0079] The actuator is preferably a high efficiency, high-bandwidth device. High efficiency allows relatively large forces to be generated without overheating. Preferably, such a device generates a force of about 2 N for a power consumption of under 5 W. Peak force in the preferred embodiment was selected to be large enough to adequately simulate a keypress effect. High bandwidth allows the force feedback to change quickly, improving the quality of haptic effects.

[0080] To apply a force to moving assembly **100**, current is driven through magnet wire **108**. The direction of the current flow determines the direction of the force. To improve efficiency, a rare earth magnet with energy density of at least about 27 million Gauss-Oersteds is preferably employed. Ferromagnetic material with a good permeability is preferably used for the flux return path to further maximize the air gap flux density. There are design tradeoffs between the air gap length, the surface area and thickness of the magnet, among other factors, which would be apparent to a practitioner skilled in the art of electromagnetic actuator design.

[0081] Each of one magnet wire **108(1)-(N)** is driven by an actuator circuit **800**, shown in FIG. 8. In one embodiment, a digital input bus 14 bits wide is shared by all of actuator circuits **800(1)-(N)**. The least significant 8 bits of the digital bus encodes the pulse width, the next 4 bits encode the haptel identifier, the next bit encodes the latch control, and the most significant bit encodes the direction of the actuation (e.g., pulling downward or pushing upward).

[0082] Comparator **805** is a 4-bit comparator. Suitable parts are available from Motorola of Schaumburg, Ill. under trade designation MC74F85. Comparator **805** continually compares the haptel identifier on the digital bus to the binary number encoded on identifier switch array **815**. Identifier switch array **815** is a 4 position DIP switch. Suitable parts are available from Grayhill of La Grange, Ill. under trade designation 76SB04. Each actuator circuit has a unique setting on its identifier switches. The four bits of identification are adequate to distinguish between the nine haptels in this embodiment. Resistor network **820** keeps comparator inputs near ground when a switch is open. Suitable parts are available from Matsushita Electric of Secaucus, N.J. under trade designation EXB-F6E222G.

[0083] The latch control bit couples to the $\bar{=}$ IN input of comparator **805**, and inverter **810** couples the logical negation of the latch control bit to the $<$ IN input. When the latch

control bit is high, the P=Q output of comparator **805** is high when the haptel identifier on the digital bus matches the number encoded on the identifier switches. When the latch control bit is low the P=Q output is low regardless of the haptel identifier on the digital bus. Inverter **810** is a standard NOT gate. Suitable parts are available from Motorola under trade designation MC74F04.

[0084] When the P=Q output on comparator **805** is high, the pulse width data is passed through latch **825** and the direction bit is passed through latch **830**. The data should remain on the digital bus until the latch bit goes low. In this way, the pulse width and direction data remain latched, and the actuator circuit can drive the magnet wire until a new value is assigned. Latch **825** and latch **830** are 8-bit latches. Suitable parts are available from Texas Instruments of Dallas, Tex. under trade designation SN74F573.

[0085] Clock **835** is a CMOS oscillator which generates a clock signal at a high frequency, preferably at least 4 MHz. Suitable parts are available from Epson America of Torrance, Calif. under trade designation SG531 P. Inverters **840** and **850** are standard NOT gates, such as the Motorola MC74F04. Inverters **840** invert the clock signal and delay the propagation of the signal. There is a brief time period during at the very beginning of each clock cycle when both inputs to AND gate **845** are high. AND gate **845** is a standard AND gate, such as the Motorola MC74F08. The output of inverter **850** is a delayed version of the original clock, due to the even number of inverters. Thus the pulse from AND gate **845** comes at the very end of the clock cycle which drives counters **855** and **860**.

[0086] Counters **855** and **860** are 4-bit synchronous counters cascaded to form an 8-bit counter. Suitable parts are available from Texas Instruments under trade designation SN74F163A. This counter freely cycles from 0 to 255, driven by the delayed clock signal. Comparators **865** and **870** are 4-bit comparators cascaded to form an 8-bit comparator. Suitable parts are available from Motorola under trade designation MC74F85. The P>Q output of comparator **870** is high when the latched pulse width value is strictly greater than the current synchronous counter value. Thus the width of the P>Q pulse is proportional to the pulse width value. If the pulse width value is 0, the P>Q output is never high. If the pulse width value is 255, the P>Q output is high for 254 out of every 255 clock cycles.

[0087] The output of AND gate **845** latches the outputs of comparator **870** and latch **830** into latch **875** at the end of each clock cycle. In this way, the output of comparator **870** is guaranteed to be valid, taking into account the propagation delays in the synchronous counters and the comparators from the beginning of the clock cycle. Latch **875** is an 8-bit latch. Suitable parts are available from Texas Instruments under trade designation SN74F573.

[0088] Motor driver chip **885** uses the pulsing comparator output to enable and disable its outputs. When **1,2EN** is high, the outputs are switched on and current can flow. When **1,2EN** are low, the outputs are in a high-impedance state and no current flows through magnet wire **108**. The direction of the current flow is determined by the **1A** and **2A** inputs. When **1A** is high, the **1Y** output is at 12 volts, and when **1A** is logic low, the **1Y** input is at ground. Likewise for the **2A** input and **2Y** output. Due to inverter **880**, the **1A** and **2A** inputs are always logically opposite. Thus when the direc-