

in technology, these devices may all be incorporated on a single chip or within some other monolithic structure carrying out the same logical functions and operations. This is likewise true of the entire system shown in FIG. 1.

[0037] While the invention has been described in detail herein in accordance with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art. Accordingly, it is intended by the appended claims to cover all such modifications and changes as fall within the true spirit and scope of the invention.

What is claimed is:

1. A method for controlling cryptographic operations in a plurality of cryptographic processors, said method comprising the steps of:

providing a plurality of instruction streams from a memory;

supplying said instruction streams to said processors initially based on location within said memory; and
retrieving subsequent instruction streams by said processors from dynamically partitioned locations in said memory assigned.

2. A method for controlling cryptographic operations comprising the step of supplying a balanced set of instruction streams from memory to a plurality of distinct cryptographic processors operating securely and in a coordinated fashion.

3. A method for controlling cryptographic operations comprising the step of supplying a balanced set of instruc-

tion streams from memory to an array of groups of cryptographic processors with the processors in each group operating securely and in a coordinated fashion.

4. The method of claim 3 in which said at least one of said cryptographic processors include a cryptographic engine capable of processing requests in a pipelined fashion.

5. The method of claim 3 in which each cryptographic processor includes a cryptographic engine, a microprocessor for controlling said engine, an interface for supplying instructions to said processor and a switch for controlling the flow of information amongst said engine, said microprocessor and said interface.

6. A system for carrying out cryptographic operations, said system comprising:

an array of groups of processors, with each of said groups including a plurality of cryptographic processors operating together and in a secure fashion; and

a source of instructions matched to the capacities of the cryptographic processors to which they are directed.

7. The system of claim 6 in which said source of instructions includes a dynamically partitioned memory.

8. The system of claim 6 in which at least one of said cryptographic processors includes a cryptographic engine capable of processing requests in a pipelined fashion.

9. The system of claim 6 in which all of said cryptographic processors include a cryptographic engine capable of processing requests in a pipelined fashion.

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