

[0029] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED  
EMBODIMENT(S)

[0030] In general, the formation of an LCD panel includes the formation of an array of thin-film transistors (TFT). The formation of a TFT array for a LCD panel is similar to the process of forming transistors in semiconductor devices, and as such, requires a highly controlled processing environment. Accordingly, forming a TFT array generally includes a series of processing operations that may include repetition of certain processes such as cleaning, masking, deposition, and etching.

[0031] As illustrated in FIG. 1A, the process of forming TFT array is initiated by placing a glass substrate 103 upon a stage 101. Typically, the process of forming LCD panels is not done on a panel-by-panel basis, but rather the process is completed on a sheet of glass which is larger than the intended LCD panel. This sheet of glass can be sectioned into smaller individual LCD panels after formation of the TFT array. Sectioning is completed after formation of the TFT array for ease of processing, consistency, and efficiency.

[0032] According to one embodiment, the glass substrate 103 can be rectangular, having a length, width, and thickness. The glass substrates are generally large, having a length of not less than about 0.5 meters. Still, the length of such glass substrates may be greater, such as not less than about 0.75 m, not less than about 1.0 m, or even not less than about 2.0 m, oftentimes within a range between about 1.0 m and about 5.0 m. The width is generally comparable to the length, such that the substrates generally have a width of not less than about 0.5 m. In other embodiments, the width of the substrates is greater, such as not less than about 0.75 m, not less than about 1.0 m, or even not less than about 1.5 m. The width of the substrates is generally within a range between about 0.5 m and about 5.0 m.

[0033] The glass substrates generally have a thickness of not greater than about 3.0 cm. In one embodiment, the thickness is less, such as not greater than about 2.0 cm, or even not greater than about 1.0 mm. Still, the thickness of the glass substrates is limited, and is typically not less than about 1.0 mm.

[0034] It will be appreciated that the process of producing most of the glass for windows (i.e., the float process) is not sufficient for producing glass substrates for LCD panels. One particular method of forming glass substrates for LCD panels is a fusion process where molten glass flows into a trough, or isopipes. Upon filling the isopipe, the molten glass flows over opposing sides of the isopipe, which is appropriately shaped such that the streams of glass fuse together and cool to form high quality glass substrates. As will be appreciated, the glass substrates generally have particular properties such as high thermal stability, and reduced levels of particular elements, such as free alkali metals and halides.

[0035] The stage 101 is provided as a support surface of the glass substrate during processing of the glass substrate. Accordingly, the stage 101 must be of comparable size to the size of the glass substrates being processed. As such, the stage 101 can have a rectangular shape, having a length and width as described above with respect to the glass substrate. Generally, the length of the stage is not less than about 0.5 meters. Still, the length of the stage may be greater, such as not less than about 0.75 m, not less than about 1.0 m, or even not less

than about 2.0 m. Generally, the length of the stage is limited, such that it is not greater than about 10 m, and particularly within a range between about 1.0 m and about 5.0 m. As such, the width of the stage can be comparable, such that the width is not less than about 0.5 m. In other embodiments, the width of the stage is greater, such as not less than about 0.75 m, not less than about 1.0 m, or even not less than about 1.5 m. The width of the stage is generally limited such that it is not greater than about 10 m and particularly within a range between about 0.5 m and about 5.0 m.

[0036] The thickness of the stage is less than the other dimensions, but generally not less than about 0.5 cm. According to one embodiment, the thickness of the stage is not less than about 0.8 cm, or even not less than about 1.0 cm. In particular, the thickness of the stage is typically within a range between about 1.0 cm and about 20 cm.

[0037] After placing the glass substrate on the stage, the processes for forming the TFT array can be initiated. In general, the glass substrate will be subjected to a plurality of processing operations, the purpose of which is to form an array of transistors, and oftentimes other electronic components, which can include for example, the electronics controlling the pixels. While transistors can have a variety of designs, the basic components are the same, and as such, formation of a transistor generally includes formation of gate electrode regions, dielectric regions, semiconducting regions, and source/drain regions and properly interconnecting each of these regions. Moreover, it will be appreciated that there are many designs for transistors, and accordingly the interconnection and placement of the regions can be changed. The following process is directed to forming a bottom gate transistor, that is the gate electrode is formed directly on the glass substrate, but it will be appreciated that other transistor designs are possible.

[0038] The process of forming the TFT array for a bottom gate designed transistor is initiated by forming a patterned array of gate electrodes and bus lines. As such, referring to FIG. 1B, a cross-sectional view of the workpiece of FIG. 1A is illustrated after forming electrodes 105 and 107. According to a particular embodiment, electrode 105 is a gate electrode and electrode 107 is a capacitor electrode. Generally, formation of the electrodes 105 and 107 is facilitated by first forming a patterned mask layer and then forming the electrodes in the voids of the patterned mask layer. Typically the patterned mask layer is a soft mask, such as a patterned mask layer formed via photolithography.

[0039] According to one embodiment, the electrodes 105 and 107 (and any bus lines) are formed by a deposition process. In particular, the deposition process can include a thin film deposition process, such as chemical vapor deposition (CVD) process, physical vapor deposition (PVD) (e.g., sputtering), atomic layer deposition (ALD), or any combination thereof. In one particular embodiment, the gate electrodes and gate bus lines are formed via plasma-enhanced CVD (PECVD).

[0040] The deposited electrodes and bus lines can be quite thin, and may include a plurality of thin films. Suitable thicknesses for the gate electrodes and bus lines can be on the order of submicron, such as not greater than about 500 nm, and particularly within a range between about 100 nm to about 300 nm.

[0041] The gate electrodes and bus lines can include a conductive material, such as a metal or metal alloy. Suitable metals can include aluminum, chromium, tantalum, tungsten,