[0075] The substrate **401** can include an inorganic material, ranging from natural materials such as stone, to fabricated materials such as a metals and metal alloys. Particularly suitable inorganic materials can include metals or ceramics, or combinations thereof. Suitable metals may include transition metals, light weight metals, or metal alloys. In one embodiment, the substrate **401** includes a metal such as aluminum, iron, chromium, steel, nickel, or combinations thereof. Particularly suitable ceramics can include oxides, nitride, or carbides. Suitable oxides can include metal oxides, particularly non-reactive and chemically stable oxides, such as for example, Al_2O_3, SiO_2, Cr_2O_3, MgO, ZrO_2, TiO_2, Y_2O_3, and Fe_2O_3.

[0076] Referring to FIG. **5**, a top view of a stage **500** is illustrated according to one embodiment. Generally, the stage is used to support the glass substrate during the formation of the TFT array and other components making the final-formed LCD. Notably, the upper surface of the stage **500** is patterned having a raised portion **501** and a recessed portion **503**. The patterned surface is illustrated as having a continues pattern such that the raised portion **501** extends in a continuous pathway along the upper surface of the stage **500**. It will be appreciated, that the pattern demonstrated in FIG. **5** is illustrative and other patterns can be formed, such as a non-continuous pathways having irregular or polygonal patterns.

[0077] Generally, the raised portions **501** defining the pattern on the upper surface of the stage **500** comprise not less than about 30% of the total surface area of the upper surface. In another embodiment, the pattern covers not less than about 50%, such as not less than about 60%, or 75%, or even not less than about 80% of the total surface area of the upper surface.

[0078] Referring to FIG. **6**, a cross-sectional view of a portion of a stage **600** is illustrated. The stage **600** includes raised portions **602** and **604**, which extend above the upper surface **603** and define recesses **606**. As used herein, the working surface **605** is defined as the surface that makes contact with a workpiece. Accordingly, in embodiments utilizing an unpatterned surface, the upper surface and the working surface are the same. However, for embodiments utilizing a patterned surface having raised portions **602** and **604** and recesses **606**, the working surface **605** is different than the upper surface **603** and the working surface **605** defines a working plane **609** that is different than the upper plane **607** defined by the upper surface.

[0079] Generally, the surface area of the working surface is not less than about 0.3 m^2. In one embodiment, the surface area of the working surface is not less than about 0.5 m^2, or not less than about 2.0 m^2, or even not less than about 4.0 m^2. Still, the surface area of the working surface is limited, such that it is typically not greater than about 25 m^2.

[0080] Notably, the working surfaces of the stages described herein have limited particle generation. Accordingly, the stages described herein include any combination of smooth working surfaces and dense structures, as structures which have rough, porous surfaces tend to generate particles which may damage the sensitive electrical components being formed. As such, generally the working surface is a smooth surface, having an average surface roughness (R_a) of not greater than about 200 microns. In one particular embodiment, the average surface roughness (R_a) is less, such as not greater than about 100 microns, or not greater than about 50 microns, or even not greater than about 10 microns. In particular, the average surface roughness (R_a) is within a range between about 100 microns and about 0.1 microns, and more particularly between about 1.0 micron and about 50 microns.

[0081] The working surface **605** of the stage **600** can have superior flatness as well. The flatness of a surface is typically understood to be the maximum deviation of a surface from a best-fit reference plane (see ASTM F 1530-02). In this regard, normalized flatness is a measure of the flatness of the surface normalized by the surface area on the generally planar surface, in this case the surface area of the working surface. According to one embodiment, the normalized flatness (nFlatness) of the generally planar surface is greater than about 10 $\mu m/cm^2$, such as not greater than about 5.0 $\mu m/cm^2$, or even not greater than about 1.0 $\mu m/cm^2$. Still, the normalized flatness of the generally planar surface can be less, such as not greater than about 0.5 $\mu m/cm^2$, or not greater than about 0.1 $\mu m/cm^2$. However, the normalized flatness of the generally planar surface is generally within a range between about 5.0 $\mu m/cm^2$ and about 0.01 $\mu m/cm^2$.

[0082] The stages provided herein, and particularly the working surfaces of such stages exhibit a reduced warping as characterized by normalized warp, hereinafter nWarp. The warp of a stage is generally understood to be the deviation of the median surface of the substrate from a best-fit reference plane (see ASTM F 697-92(99). In regards to the nwarp measurement, the warp is normalized to account for the surface area of the sapphire substrate. According to one embodiment, the nwarp is not greater than about 10 $\mu m/cm^2$, such as not greater than about 5.0 $\mu m/cm^2$, or even not greater than about 1.0 $\mu m/cm^2$.

[0083] The working surface can also exhibit reduced bow. As is typically understood, the bow of a surface is the absolute value measure of the concavity or deformation of the surface, or a portion of the surface, as measured from the substrate centerline independent of any thickness variation present. The working surface of stages provided herein exhibit a reduced normalized bow (nBow) which is a bow measurement normalized to account for the surface area of the working surface. As such, in one embodiment the nBow of the generally planar surface is not greater than about 10 $\mu m/cm^2$, such as not greater than about 5.0 $\mu m/cm^2$, or even not greater than about 1.0 $\mu m/cm^2$. According to another embodiment, the nBow of the substrate is within a range of between about 5.0 $\mu m/cm^2$ and about 0.1 $\mu m/cm^2$.

[0084] The stages provided herein can also exhibit superior parallelism. Parallelism is a measure of the average deviation in distance between two planes, and particularly the deviation in distance between a datum plane and a best fit plane of a selected surface. In reference to FIG. **6**, the stages provided herein have a parallelism as measured between a bottom surface **611** and the working surface **605** of not greater than about 1000 μm. According to another embodiment, the parallelism is less, such as not greater than about 500 μm, or not greater than about 100 μm.

[0085] FIG. **7** includes a perspective view of a LCD glass substrate effector in accordance with one embodiment. The effector **700** illustrated is a handler configured to engage and support a LCD glass substrate in transport, such as to or from a stage. As illustrated, the effector **700** can be formed such that it includes a body **701** including arm portions **703** and **705**. In particular embodiments as illustrated, the arm portions **703** and **705** can extend from the body in a direction such that they are substantially parallel to each other giving the effector a shape of a fork.