resulting product had a density of 2.75 g/cc, 15 vol % porosity, and a volume resistivity ($R_v$) of 2.0E3 Ωcm.

Comparative Example 2

**[0099]** A stage having a layered structure for forming LCD articles thereon is made using the following process. The process for forming the stage in Comparative Example 1 is followed, but after firing the green article, the fired article is coated with a layer of chemically vapor deposited (CVD) silicon carbide to form a skin layer over the substrate. The skin layer has an average thickness of 150 microns. This resulted in closing the porosity at the surface of the substrate, making the article smoother and more dense. The volume resistivity of the skin layer of the layered stage is 1.0E2 Ωcm.

**[0100]** Referring now to FIGS. **8-10**, plots are provided that illustrate the volume resistivity over a range of voltages for 17 samples made in accordance with the process of Example 1, including grinding with 320 grit to remove approximately 200 microns of material from the surface.**2**. Each of the samples were measured using a Keithley 6517A Electrometer (S/N 0776902) with Keithley Model 6524 software (Hi-R test), using two, 2.54 cm diameter conductive rubber contacts in direct contact with the samples and connected to two 2.54 cm diameter electrodes.

**[0101]** In particular, FIGS. **8-10** illustrate the volume resistivity for 17 samples measured at different voltages, wherein the plot of FIG. **8** illustrates the volume resistivity of the 17 samples measured at an applied voltage of 1 V, FIG. **9** illustrates the volume resistivity of the same 17 samples measured at an applied voltage of 10 V, and FIG. **10** illustrates the volume resistivity of the 17 samples measure at an applied voltage of 100V. The samples had resistivities within a range between 1E7 Ohm cm and 5E8 Ohm cm across the range of applied voltages, demonstrating consistent volume resistivity values suitable for ESD dissipative applications. Moreover, the samples had superior resistivity capabilities over a range of applied voltages, demonstrating the capability for dissipating electrostatic discharges occurring over a wide range of voltages.

**[0102]** While the invention has been illustrated and described in the context of specific embodiments, it is not intended to be limited to the details shown, since various modifications and substitutions can be made without departing in any way from the scope of the present invention. For example, additional or equivalent substitutes can be provided and additional or equivalent production steps can be employed. As such, further modifications and equivalents of the invention herein disclosed may occur to persons skilled in the art using no more than routine experimentation, and all such modifications and equivalents are believed to be within the scope of the invention as defined by the following claims.

**1**. A process for producing a liquid crystal display (LCD) comprising:

placing a glass substrate on a stage, the stage being electrostatic discharge (ESD) dissipative and having a surface portion that has a volume resistivity ($R_v$) within a range between about 1E5 Ωcm and about 1E11 Ωcm; and

subjecting the glass substrate to at least one processing operation of a plurality of processing operations for forming an array of electronic devices on the glass substrate.

**2-3**. (canceled)

**4**. The process of claim **1**, wherein the stage comprises a substrate and the surface portion is in the form of a skin portion overlying the substrate.

**5**. (canceled)

**6**. The process of claim **4**, wherein the skin portion is formed via a film deposition process.

**7**. The process of claim **6**, wherein the film deposition process includes a process selected from the group of processes consisting of chemical vapor deposition, plasma vapor deposition, thermal spraying, and plasma spraying.

**8-10**. (canceled)

**11**. The process of claim **1**, wherein the array of electronic devices comprises an array of thin film transistors,

**12**. The process of claim **1**, wherein the at least one processing operation comprises a deposition process.

**13**. The process of claim **12**, wherein the deposition process comprises a thin-film deposition process selected from the group of processes consisting of chemical vapor deposition (CVD), physical vapor deposition (PVD), and atomic layer deposition (ALD).

**14-16**. (canceled)

**17**. The process of claim **1**, wherein the at least one processing operation includes forming a color filter on the glass substrate

**18**. The process of claim **1**, wherein the at least one processing operation includes sectioning the glass substrate

**19**. The process of claim **1**, wherein the at least one processing operation includes forming a transparent electrode.

**20**. A LCD stage comprising:

a body comprising a surface portion, the surface portion being an electrostatic discharge (ESD) diccipative material having a volume resistivity ($R_v$) within a range between about 1E5 Ωcm and about 1E11 Ωcm.

**21**. (canceled)

**22**. The LCD stage of claim **20**, wherein the body comprises a substrate and the surface portion is in the form of a skin portion.

**23**. The LCD stage of claim **22**, wherein the skin portion is in direct contact with the substrate.

**24-25**. (canceled)

**26**. The LCD stage of claim **22**, wherein the skin portion comprises silicon carbide.

**27**. The LCD stage of claim **20**, wherein the surface portion comprises an upper surface.

**28**. The LCD stage of claim **27**, wherein the upper surface comprises a pattern defined by raised portions above recessed portions, wherein the raised portions define a working surface.

**29-30**. (canceled)

**31**. The LCD stage of claim **28**, wherein the working surface has an average surface roughness ($R_a$) of not greater than about 200 microns.

**32**. (canceled)

**33**. The LCD stage of claim **28**, wherein the body comprises a bottom surface defining a bottom plane opposite the working the plane.

**34**. The LCD stage of claim **33**, wherein the body comprises a parallelism between the working surface and the bottom surface of not greater than about 1000 μm.

**35-40**. (canceled)

**41**. A method of transporting a glass substrate for LCD processing comprising:

placing a glass substrate on an effector, the effector comprising a body having an arm portions extending from