

signal line exceeds 200 pF when original electrostatic capacitance of Cs (a capacitor to be detected: a microphone in the present embodiment) is 20 pF, the detection sensitivity becomes much worse. Also, when the said Cs is checked with a few other electrostatic capacitance values, their results tend to be the same.

[0046] Additionally, both of the capacitance Cf, which is the first impedance element, and the capacitor Cs are a capacitance element connected to the signal line in this circuit, so that the same result as above is expected for calculation of both of the elements.

[0047] From these experimental results and experiences, it was found out that good detective sensitivity is secured when the capacitor to be detected, the first impedance element and the impedance converter are located closely in a way that the stray capacitance of the signal line does not exceed ten times as much as the capacitance value of the relevant Cs or Cf.

[0048] FIG. 3 A through E show specific circuit examples of the impedance converter 16 in the electrostatic capacitance detection circuit 10 shown in FIG. 2. FIG. 3 A shows a voltage follower using an operational amplifier 100. An inverting input terminal and an output terminal of the operational amplifier 100 are short-circuited. When a non-inverting input terminal of this operational amplifier 100 is an input of the impedance converter 16, and the output terminal of the operational amplifier 100 is an output of the impedance converter 16, the impedance converter 16 of which input impedance is extremely high and voltage gain A is 1 can be obtained.

[0049] FIG. 3 B shows a non-inverting amplifier circuit using an operational amplifier 101. A resistance (R10) 110 is connected between an inverting input terminal of the operational amplifier 101 and a ground, and a feedback resistance (a resistance (R11) 33) is connected between the inverting input terminal and an output terminal of the operational amplifier 101. When a non-inverting input terminal of this operational amplifier 101 is an input of the impedance converter 16, and the output terminal of the operational amplifier 101 is an output of the impedance converter 16, the impedance converter 16 of which input impedance is extremely high and voltage gain A is $(R10+R11)/R10$ can be obtained.

[0050] FIG. 3 C shows a circuit where a buffer of CMOS structure is added to an input side of the operational amplifier as shown in FIG. 3 A or B. As illustrated in the diagram, N type MOSFET 34 and P type MOSFET 35 are connected between positive and negative power supplies in series via the resistance 112 and 113, and an output of the buffer is connected to an input of the operational amplifier 100 (or 101). When the input of this buffer is an output of the impedance converter 16, and the output terminal of the operational amplifier is an output of the impedance converter 16, the impedance converter 16 of which impedance is extremely high can be obtained.

[0051] FIG. 3 D shows a circuit like the buffer at the input side in FIG. 3 C. As shown in the diagram, N type MOSFET 34 and P type MOSFET 35 are connected between positive and negative power supplies are connected in series, and outputs are made from connection points of both MOSFET.

[0052] FIG. 3 E is a circuit where a non-inverting input of an operational amplifier 102 is an input of the impedance converter, an inverting input terminal of the operational amplifier 102 is connected to one end of a resistance 114, and an output and the inverting input of the operational amplifier 102 are connected via a resistance 115. As indicated in FIG. 3 D and E, having these types of structure realizes the impedance converter 16 of which input impedance is extremely high.

[0053] (Second Embodiment)

[0054] The following describes an electrostatic capacitance detection circuit according to a second embodiment of the present invention.

[0055] FIG. 4 is a circuit diagram of an electrostatic capacitance detection circuit 30 in the second embodiment. This electrostatic capacitance detection circuit 30 is roughly composed of a core unit 31 equivalent to the electrostatic capacitance detection circuit 10 shown in FIG. 2, an inverting unit 32 that receives signal voltage V01 at a signal output terminal 20 of the core unit 31 as an input and inverts the signal voltage V01, an adding unit 33 that adds up signal voltage V03 at an output terminal 23 of the inverting unit 32 and signal voltage V02 at an AC output terminal 22 of the core unit 31 and outputs a detection signal of voltage V04 to an output terminal 24.

[0056] The core unit 31 has the same circuit as the electrostatic capacitance detection circuit 10 shown in FIG. 2. Therefore, according to the above expression 5, the voltage V01 of the signal output terminal 20 of the core unit 31 is as follows:

$$V01 = -(1 + Cs/Cf) \cdot (R2/R1) \cdot (Vin/A) \quad (\text{Expression 6})$$

[0057] According to the above expression 1, the voltage V02 of the AC output terminal 22 of the core unit 31 is as follows:

$$V02 = -(R2/R1) \cdot (Vin/A) \quad (\text{Expression 7})$$

[0058] The inverting unit 32 is an inverting amplification circuit comprising a variable resistance (R4) 40, a resistance (R5) 41, a variable resistance (R6) 42, a capacitor 43 and an operational amplifier 44, of which voltage gain is -1, and resistance values of the variable resistance (R4) 40 and the variable resistance (R6) 42 are adjusted to have a phase of the signal V03 at the output terminal 23 identical to the one of the signal V02 at the AC output terminal 22 of the core unit 31. Therefore, the following relation is ideally established between the input voltage V01 and the output voltage V03 of this inverting unit 32.

$$V03 = -V01 \quad (\text{Expression 8})$$

[0059] The adding unit 33 is an adding device of which three resistances (R7) 45, (R8) 46 and (R9) 47 having the same resistance value are connected to an operational amplifier 48. So, the following relation is established among two input signals of the voltage V02 and the voltage V03 and the output voltage V04.

$$V04 = -(V02 + V03) \quad (\text{Expression 9})$$

[0060] After the above expression 8 is assigned to this expression 9 and V03 is deleted, the above expressions 6 and 7 are assigned to it. Then, the following expression becomes effective.