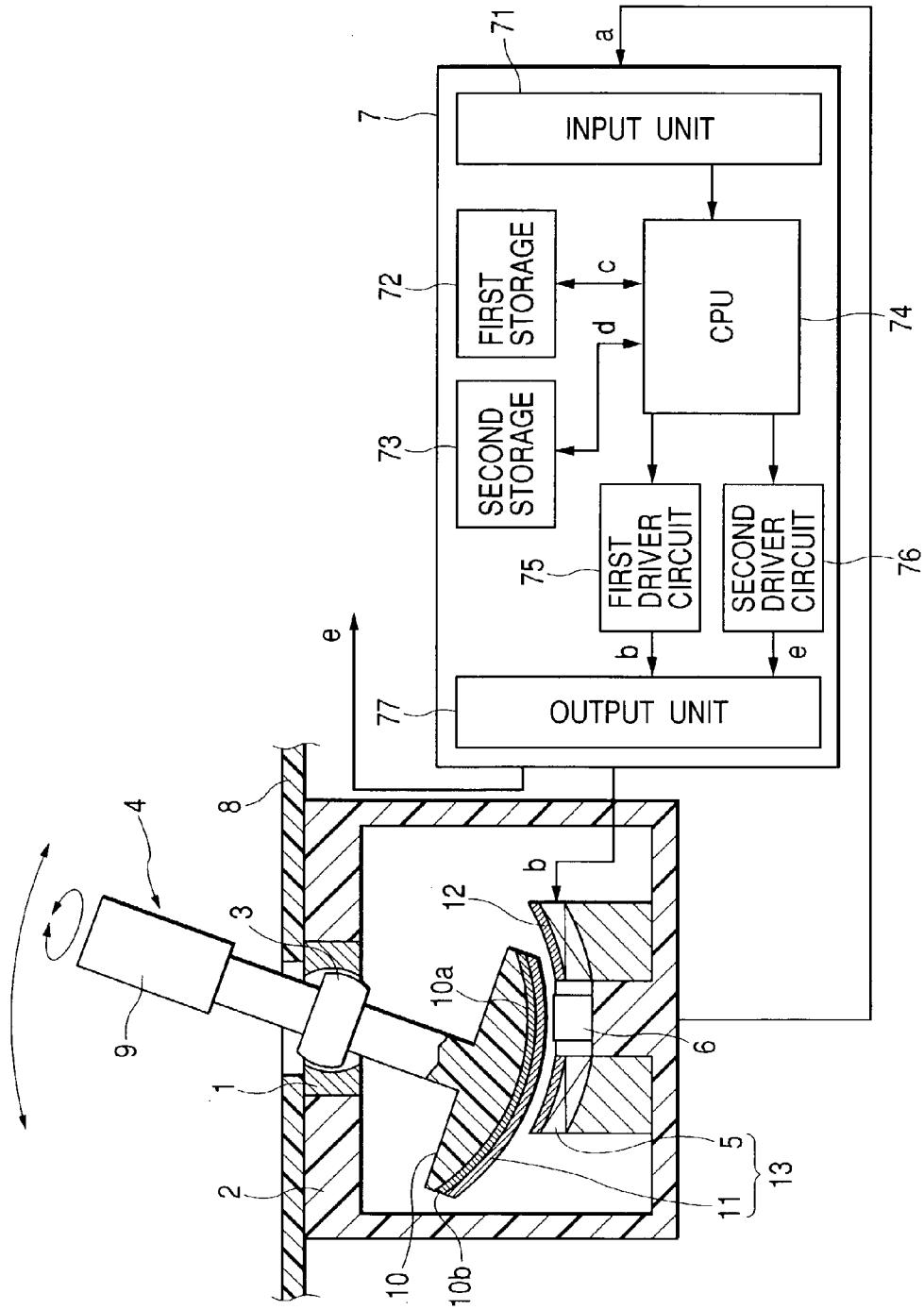
FIG. 3


INPUT UNIT
FIRST STORAGE
SECOND STORAGE
CPU
FIRST DRIVER CIRCUIT
SECOND DRIVER CIRCUIT
OUTPUT UNIT
a
b
c
d
e
1
2
3
4
5
6
7
8
9
10
10a
10b
11
12
13
71
72
73
74
75
76
77