include a serializer (SER). The DSI host **1111** of the application processor **1110** may perform a serial communication with the DSI device **1151** of the display **1150** through a display serial interface (DSI).

[0138] In some embodiments, the DSI host **1111** may include a serializer (SER), and the DSI device **1151** may include a deserializer (DES). The computing system **1100** may further include a radio frequency (RF) chip **1160** that can communicate with the application processor **1110**. The PHY **1113** of the computing system **1100** and the PHY **1161** of the RF chip **1160** may transmit and receive data according to MIPI (Mobile Industry Processor Interface) DigRF. The application processor **1110** may further include a DigRF MASTER **1114** that controls the transmission and reception of data according to the MIPI DigRF.

[0139] Meanwhile, the computing system **1100** may include a global positioning system (GPS) **1120**, a storage **1170**, a mic **1180**, dynamic random access memory (DRAM) **1185**, and a speaker **1190**. The computing system **1100** may perform a communication using an ultra wideband (UWB) **1210**, a wireless local area network (WLAN) **1220**, and a worldwide interoperability for microwave access (WIMAX) **1230**. However, the configuration of the computing system **1100** and the interface illustrated in FIG. **12** are examples, and at least some example embodiments of the inventive concepts are not limited thereto.

[0140] It will understood to those skilled in the art that the data encoding apparatus can be realized in the form of systems, methods, and other products including a computer-readable program code stored in a computer-readable medium. The computer-readable recording medium may be any type of medium provided in an instruction execution system, equipment or device or connected thereto to store or include program.

[0141] Example embodiments of the inventive concepts having thus been described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the intended spirit and scope of example embodiments of the inventive concepts, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

1. A data encoding apparatus, comprising:

a memory storing computer-readable instructions; and

one or more processors configured to execute the computer-readable instruction such that the one or more processors are configured to,

receive first video data in a macroblock unit,

determine a first rounding offset value using the first video data,

create second video data by applying the first rounding offset value to the first video data,

determine a second rounding offset value, which is different from the first rounding offset value, using the second video data, and

create a quantized coefficient by applying the second rounding offset value to the first video data.

2. The data encoding apparatus of claim **1**,

wherein the one or more processors are configured to execute the computer-readable instruction such that the one or more processors are configured to determine the first rounding offset value depending on a prediction mode or a level value.

3. The data encoding apparatus of claim **2**,

wherein the one or more processors are configured to execute the computer-readable instruction such that the one or more processors are configured to determine the second rounding offset value using the number of data having a level value of 0 between first data and second data.

4. The data encoding apparatus of claim **3**, further comprising:

one-dimensionally arranging the second video data,

wherein the first data is final data having a level value of not 0 in the one-dimensionally arranged second video data.

5. The data encoding apparatus of claim **4**,

wherein the second data is data that has a level value of not 0 and is nearest to the first data in the one-dimensionally arranged second video data.

6. The data encoding apparatus of claim **1**,

wherein the one or more processors are configured to execute the computer-readable instruction such that the one or more processors are configured to determine the first or second rounding offset value using a previously stored lookup table.

7. The data encoding apparatus of claim **1**,

wherein the one or more processors are further configured to execute the computer-readable instruction such that the one or more processors are configured to calculate the first or second rounding offset value depending on a first equation.

8. (canceled)

9. The data encoding apparatus of claim **1**,

wherein the first video data is data transformed into a frequency domain.

10. The data encoding apparatus of claim **1**,

wherein the macroblock unit includes 4×4 pixel or 16×16 pixel.

11. A data encoding apparatus, comprising:

a memory storing computer-readable instructions; and

one or more processors configured to execute the computer-readable instruction such that the one or more processors are configured to,

receive 1st to n^{th} video data,

determine 1st to n^{th} quantized coefficients based on the 1st to n^{th} video data, n being a natural number equal to or greater than 2,

determine 1st to n^{th} rounding offset values based on the 1st to n^{th} quantized coefficients,

determine 1st to n^{th} transformed quantized coefficients by applying the 1st to n^{th} rounding offset values to the 1st to n^{th} quantized coefficients, and

one-dimensionally arrange the 1st to n^{th} transformed quantized coefficients depending on a first rule.

12. The data encoding apparatus of claim **11**,

wherein the one or more processors are configured to execute the computer-readable instruction such that the one or more processors are configured to determine additional rounding offset values using the one-dimensionally arranged 1st to n^{th} transformed quantized coefficients.

13. The data encoding apparatus of claim **12**,

wherein the one or more processors are configured to execute the computer-readable instruction such that the one or more processors are configured to determine the additional rounding offset values by using a final k^{th}