base region (**75**) of a third doping density located between the emitter region and the collector region, and a further region (**85**) of a fourth doping density located between the base region (**75**) and the collector region (**86**), wherein at least the further region (**85**) extends to an overlying dielectric-semiconductor interface (**791**), and wherein the base region (**75**) has a first dopant boundary (**751**) with the further region (**85**) and the collector region (**86**) has a second dopant boundary (**861**) with the further region (**85**) and wherein at least one (**751** or **861**) of the first (**751**) and second (**861**) dopant boundaries has a maximum dopant density at a distance Y>0 beneath the dielectric-semiconductor interface (**791**). According to a further embodiment, Y≧0.1 micrometers. According to a still further embodiment, the first (**751**) and second (**861**) dopant boundaries have maximum dopant concentrations at distances Y**1** and Y**2**, respectively, beneath the dielectric-semiconductor interface (**791**), and wherein Y**1**>0 and Y**2**>0. According to a still further embodiment, the base region (**75**) and the collector region (**86**) are more heavily doped than the further region (**85**). According to a yet further embodiment, a peak dopant concentration of the base region (**75**) and a peak dopant concentration of the collector region (**86**) exceed an average dopant concentration of the further region (**85**) by at least a factor of 5. According to a still yet further embodiment, the peak dopant concentration of the base region (**75**) and the peak dopant concentration of the collector region (**86**) exceed the average dopant concentration of the further region (**85**) by at least a factor of 10. According to a yet still further embodiment, the emitter region (**78**) and a base contact region (**77**) are substantially shorted together. According to another embodiment, the first (**751**) and second (**861**) dopant boundaries are separated by a minimum distance D through the further region (**85**), and wherein the minimum distance D occurs at a depth Y>0 beneath the dielectric-semiconductor interface (**791**). According to a still another embodiment, the bipolar transistor electrostatic discharge (ESD) clamp (**21**, **21'**, **70**, **700**) is adapted to have an avalanche trigger voltage Vt**1** substantially determined by D.

[0044] According to a second embodiment, there is provided a method for forming a bipolar transistor electrostatic discharge (ESD) clamp (**21**, **21'**, **70**, **700**), comprising, providing a semiconductor substrate (**72**) having a first region (**74**) of a first conductivity type or a second conductivity type and first and second dopant density, respectively, extending to a first surface (**71**), forming a first WELL region (**762**, **86**) of a third conductivity type and third doping density extending from the first surface (**71**) into the first region (**74**) and having a first lateral boundary (**927-1**, **861**), forming a second WELL region (**75**) of a fourth conductivity type opposite the third conductivity type and having a fourth doping density extending into the first WELL region and having a second lateral boundary (**751**) separated from the first lateral boundary (**927-1**, **861**) by a minimum distance D across an intermediate portion (**85**) of the first region (**74**) having a fifth dopant density, forming a dielectric-semiconductor interface (**791**) overlying at least the intermediate portion (**85**), and wherein either: (i) the minimum distance D is located beneath the dielectric-semiconductor interface (**791**) by a distance Y>0, or (ii) the third and fourth doping densities exceed the fifth doping density at a distance Y>0 below the dielectric-semiconductor interface (**791**) by at least a factor of 5, or (iii) both (i) and (ii). According to a still further embodiment, Y≧0.1 micrometers. According to a yet further embodiment, Y≧0.2 micrometers. According to a still yet further embodiment, the third and fourth doping densities exceed the fifth doping density at a distance Y below the dielectric-semiconductor interface (**791**) by at least a factor of 10. According to a yet still further embodiment, the step of providing a semiconductor substrate (**72**) comprises providing a semiconductor substrate that has first (**74**) and second (**74**R) laterally arranged regions of a first or second conductivity type extending to a first surface (**71**), and wherein the step of forming a first WELL region (**762**, **86**) comprises forming a first WELL region (**762**, **86**; **762**R, **86**R) of a third conductivity type and third doping density extending from the first surface (**71**) between the first (**74**) and second (**74**R) laterally arranged regions, so that the first WELL region (**762**, **86**, **762**R, **86**R) and has a first lateral boundary (**861**) in the first (**74**) region and a second lateral boundary (**861**R) in the second region (**74**R), and wherein the step of forming a second WELL region comprises forming first and second spaced-apart second WELL regions (**75**, **75**R) of a fourth conductivity type opposite the third conductivity type and having a fourth doping density and extending, respectively, into the first (**74**) and second (**74**R) regions, wherein the first (**75**) of the second WELL regions has a third lateral boundary (**751**) spaced apart from the first lateral boundary (**861**) by a distance D across a first intermediate portion (**85**) of the first region (**74**) having the fifth dopant density, and the second (**75**R) of the second WELL regions has a fourth lateral boundary (**751**R) spaced apart from the second lateral boundary (**861**R} by a distance DR across a second intermediate portion (**85**R) of the first region (**74**R) having the fifth doping density, and wherein the step of forming a dielectric-semiconductor interface (**791**), comprises forming a dielectric-semiconductor interface (**791**) overlying the first intermediate portion (**85**) and forming a dielectric-semiconductor interface (**791**R) overlying the second intermediate portion (**85**R); and wherein the distances D and DR are located beneath the dielectric-semiconductor interfaces (**791**, **791**R), respectively, by depths Y_D>0 and Y_{DR}>0, respectively. According to another embodiment, D and DR are substantially equal. According to a still another embodiment, the method further comprises providing first (**78**) and second (**78**R) contact regions of the third conductivity type and third (**77**) and fourth (**77**R) contact regions of the fourth conductivity type in the first (**75**) and second (**75**R) spaced apart second WELL regions, wherein the first (**78**) and third (**77**) contact regions are coupled together and to a first terminal (**23**) of the bipolar transistor electrostatic discharge (ESD) clamp (**21**, **21'**, **70**, **700**) and the second (**78**R) and fourth (**77**R) contact regions are coupled together and to a second terminal (**22**) of the bipolar transistor electrostatic discharge (ESD) clamp (**21'**, **700**).

[0045] According to a third embodiment, there is provided a bipolar transistor electrostatic discharge (ESD) clamp (**21**, **21'**, **70**, **700**) formed in a substrate (**72**) having a first surface (**71**), and coupled to first (**23**) and second (**22**) terminals, and comprising, an emitter (**78**) coupled to the first terminal (**23**), a collector (**86**, **762**) coupled to the second terminal (**22**), a base (**75**) located between the emitter (**78**) and the collector (**86**, **762**) and an intermediate semiconductor portion (**85**) coupled between the base (**75**) and the collector (**86**, **762**) and more lightly doped than the base (**75**) and the collector (**86**, **762**), wherein at least the intermediate semiconductor portion (**85**) extends to a dielectric-semiconductor interface (**791**) at or near the first surface (**71**), and wherein the intermediate semiconductor portion (**85**) has a first interface (**751**) with the base (**75**) and second interface (**861**) with the collector (**86**,