

**[0018]** FIG. 9 schematically illustrates a cross-sectional view of one embodiment of a dielectric layer mechanically attaching the compound semiconductor devices to the receiving substrate.

**[0019]** FIG. 10 schematically illustrates a cross-sectional view of one embodiment of a second set of devices attached to the compound semiconductor devices.

**[0020]** FIG. 11 schematically illustrates a cross-sectional view of one embodiment of metal contacts applied to compound semiconductor devices.

**[0021]** FIG. 12 schematically illustrates a cross-sectional view of one embodiment in which trenches are formed between devices of a receiving substrate.

**[0022]** FIG. 13 schematically illustrates a cross-sectional view of one embodiment of a handle substrate attached to compound semiconductor devices.

**[0023]** FIG. 14 schematically illustrates a cross-sectional view of one embodiment in which a completed device is released from a receiving substrate.

**[0024]** FIG. 15 schematically illustrates a cross-sectional view of one embodiment in which receiving structure and compound semiconductor devices are attached to opposite sides of a receiving substrate.

**[0025]** FIG. 16 is a flow diagram of one embodiment of a method of processing devices on a receiving substrate.

#### DETAILED DESCRIPTION

**[0026]** In this section we shall explain several preferred embodiments of this invention with reference to the appended drawings. Whenever the shapes, relative positions and other aspects of the parts described in the embodiments are not clearly defined, the scope of the invention is not limited only to the parts shown, which are meant merely for the purpose of illustration. Also, while numerous details are set forth, it is understood that some embodiments of the invention may be practiced without these details. In other instances, well-known structures and techniques have not been shown in detail so as not to obscure the understanding of this description.

**[0027]** FIG. 1 schematically illustrates a cross-sectional view of one embodiment of a donor substrate. Donor substrate 102 may be any type of donor substrate capable of forming a semiconductor device thereon. Representatively, in one embodiment, donor substrate 102 is a wafer made of a compound semiconductor material capable of creating a semiconductor device made of a similar material. For example, donor substrate 102 is made of a group III-V semiconductor material such that a semiconductor device made of a III-V semiconductor material can be epitaxially grown thereon. In one embodiment, the III-V semiconductor material is a compound material such as gallium arsenide (GaAs) or indium gallium phosphide (InGaP). Although specific group III-V semiconductor materials are disclosed, it is contemplated that any semiconductor material may be used. In still further embodiments, the donor substrate 102 may be made of a non-compound semiconductor material capable of forming a semiconductor device thereon. For example, in one embodiment, donor substrate 102 is a non-compound material other than silicon, for example, a group IV material such as silicon (Si) or germanium (Ge).

**[0028]** A sacrificial release layer 104 may be deposited on top of donor substrate 102. Release layer 104 may be made of any material capable of being removed by an etchant that will not substantially remove a protective layer formed on the

semiconductor device. Representatively, in one embodiment, release layer 104 may be made of aluminum indium phosphide (AlInP) and, during a later step, etched using hydrogen chloride (HCl). Alternatively, release layer 104 may be made of silicon (Si) and removed with xenon difluoride (XeF<sub>2</sub>). In still further embodiments, release layer 104 can be made of any material that is different from the protective material, for example, amorphous-Si, porous silicon or spin-on glass. Release layer 104 may be grown over donor substrate 102 using a molecular beam epitaxy (MBE) or metallo-organic chemical vapor deposition (MOCVD) growth process. Alternatively, release layer 104 may be formed by other material deposition processes such as chemical vapor deposition (CVD) or physical vapor deposition (PVD) (e.g. sputtering).

**[0029]** FIG. 2 schematically illustrates a cross-sectional view of one embodiment of a device layer formed on donor substrate 102. Device layer 202 may be formed on donor substrate 102 after the formation of release layer 104 such that release layer 104 is between compound device layer 202 and donor substrate 102. Device layer 202 may be made of a compound semiconductor material, which in some embodiments, is the same material as donor substrate 102. Representatively, donor substrate 102 may be made of a III-V semiconductor material and device layer 202 may also be a III-V semiconductor material. In one embodiment, device layer 202 is grown over donor substrate 102 using a molecular beam epitaxy (MBE) or metallo-organic chemical vapor deposition (MOCVD) growth process. Alternatively, device layer 202 may be made of a single semiconductor material, for example a group IV semiconductor material such as Ge. Device layer 202 may be made of multiple layers or may be a single layer of semiconductor material. An overall thickness of compound semiconductor device layer 202 may be from about 0.5 microns (μm) to about 5 μm.

**[0030]** Once device layer 202 is formed, compound semiconductor devices 302 may be formed from device layer 202 as illustrated in FIG. 3. Compound semiconductor devices 302, may be, for example, cells having the same or different functionalities. Although devices 302 are referred to as “compound” devices, it is contemplated that compound semiconductor devices 302 are not necessarily made of compound materials. Rather, compound devices 302 may be made of a compound semiconductor material or a single semiconductor material, depending upon the material of device layer 202, as previously discussed. Compound semiconductor devices 302 may be formed by etching trenches 304 down to release layer 104. For example, although not shown, a mask layer (e.g. an oxide layer) may be formed over device layer 202 and patterned to include openings over portions of device layer 202 where trenches 304 are to be formed. A chemical etch (e.g., wet etch or plasma etch) may then be performed to etch through device layer 202. Trenches 304 may extend through an entire thickness of device layer 202 and stop at release layer 202. Alternatively, trenches 304 may be etched through release layer 202.

**[0031]** Next, dielectric layer 402 is formed over compound semiconductor devices 302 as illustrated in FIG. 4. Dielectric layer 402 may also be formed over portions of release layer 104 which are exposed between compound semiconductor devices 302. Dielectric layer 402 may be formed according to any suitable technique, for example, a plasma enhanced chemical vapor deposition technique.

**[0032]** Dielectric layer 402 serves several purposes. Representatively, dielectric layer 402 helps to bond compound