

semiconductor devices **302** to a receiving structure as will be described in more detail below. Also, as can be seen from FIG. 4, dielectric layer **402** covers all exposed surfaces of compound semiconductor devices **302**. Dielectric layer **402** can therefore also serve as a passivation and sidewall protection layer during etching of release layer **104** as will also be described in more detail below. Dielectric layer **402** may be made of any type of material suitable for serving at least these purposes. Representatively, in one embodiment, dielectric layer **402** may be made of silicon nitride or silicon oxide. In one embodiment, dielectric layer **402** may be a relatively thin layer such that it does not substantially affect the passage of light between compound semiconductor devices **302** and the associated receiving structure. For example, dielectric layer **402** may have a thickness of from about 0.01  $\mu\text{m}$  to about 1  $\mu\text{m}$ . The thickness of dielectric layer **402** may be selected depending upon the desired characteristics of compound semiconductor devices **302**. Representatively, a thinner layer may be selected where the optical characteristics of compound semiconductor devices **302** are critical and a thicker layer may be selected where the electrical characteristics of compound semiconductor devices **302** are more important.

[0033] Portions of dielectric layer **402** between each of the compound semiconductor devices **302** are etched to expose release layer **104** as illustrated in FIG. 5. Representatively, in one embodiment, a masking layer is applied over compound semiconductor devices **302** and a chemical etch (e.g., wet etch or plasma etch) is used to remove the unmasked portions of dielectric layer **402**. An example, of a masking layer is an oxide layer that is patterned such that portions of dielectric layer **402** to be removed are exposed. Exposing release layer **104** facilitates removal of release layer **104** during a later processing step.

[0034] Once compound semiconductor devices **302** are formed on donor substrate **102**, donor substrate **102** and compound semiconductor devices **302** are flipped and bonded to the top of receiving structure **602** as illustrated in FIG. 6. Receiving structure **602** may be made of a material other than that of compound semiconductor devices **302**. Representatively, where compound semiconductor devices are made of a III-V semiconductor material, receiving structure **602** may be made of silicon. Receiving structure **602** may include receiving devices **610** formed therein which are aligned with and bonded to respective compound semiconductor devices **302**. Receiving devices **610** may be silicon semiconductor devices capable of a different functionality than compound devices **302**. For example, receiving devices **610** may be fabricated to have microelectronic functionalities while compound semiconductor devices **302** can be fabricated to have optoelectronic functionalities. More specifically, in one embodiment, compound semiconductor devices **302** may have the ability to absorb, generate and modulate different wavelengths of light or generate a piezoelectric response to a mechanical input while receiving devices **610** do not have such functionalities. A dielectric layer **608** may be formed over each of receiving devices **610** to facilitate the bonding process.

[0035] The bonding process will now be described in more detail. In one embodiment, a surface activation (plasma) process is performed on compound semiconductor devices **302** according to recognized techniques. A surface activation process may further be performed on receiving devices **610**. After the activation, compound semiconductor devices **302** are aligned and brought into contact with receiving devices **610**. Chemical bonding between compound semiconductor

devices **302** and receiving devices **610** occurs through hydrogen bonding and van der Waals forces between the dielectric layer **402** on compound semiconductor devices **302** and a dielectric layer formed over receiving devices **610**. In one embodiment, bonding occurs at room temperature. Representatively, room temperature may be considered a temperature of from about 15 to about 30 degrees Celsius, for example, from 20 to 25 degrees Celsius, or about 23 degrees Celsius. The ability to bond the devices together at room temperature is important because, in embodiments where dielectric layer **402** on compound semiconductor devices **302** and the dielectric layer on receiving devices **610** are made of different materials (e.g. silicon dioxide and silicon nitride), the coefficient of thermal expansion between the dissimilar materials is not the same. Furthermore, the coefficient of thermal expansion of the donor and receiving substrates may have different coefficients of thermal expansion which can cause problems with bonding if the bonding is not done at room temperature. In addition, typical bonding procedures which occur at elevated temperatures can create stress on the device. The ability to bond at room temperature eliminates this stress.

[0036] It is recognized that for bonding to occur repeatedly and reliably, the surfaces of compound semiconductor devices **302** and receiving devices **610**, having the dielectric layer formed thereon, should be cleaned (no particulates) and smooth (less than a few nm rms roughness).

[0037] After the room temperature bonding step, a high temperature annealing process may be used to transform the bonds between the two surfaces into covalent bonds. Representatively, the bonded compound semiconductor devices **302** and receiving devices **610** can be annealed by heating to a temperature between about 150 degrees Celsius and 600 degrees Celsius to strengthen the bond.

[0038] In some embodiments, compound semiconductor devices **302** and receiving devices **610** are clamped together under a mechanical load to facilitate the bonding step. Alternatively, no external load is applied depending on the characteristics of the material stack and coefficient of thermal expansion (CTE) mismatches between compound semiconductor devices **302** and receiving devices **610**.

[0039] As further illustrated in FIG. 6, receiving structure **602** is attached to receiving substrate **604** along a surface opposite compound semiconductor devices **302**. An optional release layer **606** may further be formed between receiving structure **602** and receiving substrate **604** to facilitate removal of receiving substrate **604**.

[0040] In one embodiment, receiving substrate **604** is a structured wafer that includes multiple through holes (e.g., holes **612**) (not drawn to scale) that form a pattern on the top surface of receiving substrate **604**. Each of holes **612** extends vertically through the thickness of receiving substrate **604**. In one embodiment, holes **612** can be formed with uniform spacing among them, with non-uniform spacing among them, or at random locations. Holes **612** can be of the same size or different sizes (e.g., a diameter in the range of 50-500 microns ( $\mu\text{m}$ )). In one embodiment, receiving substrate **604** is made of silicon or any silicon-based materials. It is appreciated that receiving substrate **604** can be single crystalline or polycrystalline silicon. In alternative embodiments, receiving substrate **604** can be made of other materials such as ceramic materials. In one embodiment, various additional layers cover the entire surface of receiving substrate **604**. It is appreciated that the shape and dimensions of receiving substrate **604** will