

be dictated, in one embodiment, by the requirements of receiving structure 602 adhered to receiving substrate 604.

[0041] Receiving substrate 604 can be manufactured with standard semiconductor processing techniques. In one embodiment, receiving substrate 604 can be formed from a base wafer (e.g., a silicon wafer) with a hard mask deposited thereon. An example of the hard mask is an oxide layer that is patterned to define the size(s) and locations of holes 612. The hard mask exposes the part of the silicon wafer where holes 612 are to be formed. An etchant or a plasma process can then be used to etch through the silicon wafer to form holes 612. The hard mask is removed after holes 612 are formed. A dielectric layer 614 (e.g., an oxide layer and/or a nitride layer) is formed on the entire exposed surface (including the inner surfaces of holes 612 (i.e., the surface that defines the passage or lumen)) of receiving substrate 604, as shown in FIG. 6. In one embodiment, dielectric layer 614 is a thin layer of silicon dioxide with a thickness in the range of 1000 Angstroms-1 micron. It is noted that receiving substrate 604 is formed prior to application of receiving structure 602. Still further, although a structured receiving substrate 604 is described and illustrated it is contemplated that receiving substrate 604 may be any standard, non-structured wafer suitable for processing of a receiving structure 602 and any associated components as described herein. For example, in another embodiment, receiving substrate 604 is solid, without through holes 612.

[0042] It is important to note that the features on the surfaces of compound devices 302 and receiving devices 610 are critical to allow the hydrogen gas that is evolving during the bonding process to escape and not cause bonding defects. In particular, during the bonding process certain gases (e.g., hydrogen) may be generated at the surface-to-surface contact ("interface") due to chemical reactions. If the gas is left at this interface, it will migrate and can turn into gas pockets. These gas pockets can become defects, which prevent bonding of the devices. The through passages within receiving substrate 604 as described herein provide a route for the gas such that it can escape the interface.

[0043] Once compound semiconductor devices 302 are bonded to receiving devices 610, release layer 104 is removed so that donor substrate 402 can be separated from compound semiconductor devices 302 as illustrated in FIG. 7. In one embodiment, a chemical etching process (e.g., wet etch or plasma etch) is used to remove release layer 104. In one embodiment, HCl or XeF₂ can be used as an etchant. Since receiving devices 610 and compound semiconductor devices 302 are coated all around their surfaces with dielectric layers 608 and 402, respectively, which are made of a material that is not etched by the etchant, they are not affected by the etchant. Only release layer 104 is exposed to the etchant and will be etched away. The presence of the exposed surfaces between compound semiconductor devices 302 allows the etchant to reach release layer 104. It is further contemplated, that in some embodiments, to accelerate the release process, donor substrate 402 may have a structure similar to receiving substrate 604 such that there are holes through which the etchant can pass to reach release layer 104 from its bottom surface. It is also contemplated that neither donor substrate 402 nor receiving substrate 604 is required to have through holes through which the etchant can pass to accomplish the etching.

[0044] It should be understood that the choice of chemical composition of the release layer 104 is selected so that etching of the release layer 104 does not substantially attack or dam-

age any other layers, particularly, dielectric layers 402, 608. Representatively, as previously discussed, release layer 104 may be made of aluminum indium phosphide (AlInP) and etched using hydrogen chloride (HCl). Alternatively, release layer 104 may be made of silicon (Si) and removed with xenon difluoride (XeF₂). Both HCl and XeF₂ are selective etchants in that they will not remove the silicon nitride or oxide dielectric layers 402, 608.

[0045] In still further embodiments, release layer 104 can be made of spin-on glass, amorphous-Si or porous silicon and dielectric layer 402 can be made of oxide. In other embodiments, release layer 104 is made of oxide and dielectric layer 402 can be made of amorphous-Si or Si-nitride.

[0046] In one embodiment, after compound semiconductor devices 302 are released, donor substrate 102 can be cleaned for reuse. Compound semiconductor devices 302 remain attached to receiving devices 610 as illustrated in FIG. 8 with a bottom surface 802 exposed. A further dielectric layer 902 is then applied over each of compound semiconductor devices 302 and receiving structure 602 as illustrated in FIG. 9. Dielectric layer 902 may be substantially the same as dielectric layer 402 and applied in a similar manner. Dielectric layer 902 covers exposed surface 802 of compound semiconductor devices 302 such that all surfaces of compound semiconductor devices 302 are covered. Additionally, dielectric layer 902 acts to mechanically attach compound semiconductor devices 302 to receiving devices 610 to further reinforce the bonding between the two structures. In this aspect, the initial bonding strength between compound semiconductor devices 302 and receiving devices 610 does not need to be extremely high since a mechanical bonding step, through the encapsulation by dielectric layer 902, is also performed. Although the dielectric encapsulation is not a necessary part of the invention for bond strength or utility of the bonded structures.

[0047] A second set of compound semiconductor devices 1002 may also be bonded to the first set of compound semiconductor devices 302 and covered with a further dielectric layer 1004 as illustrated in FIG. 10. Compound semiconductor devices 1002 may be formed and bonded to compound semiconductor devices 302 using substantially the same process steps previously discussed with reference to FIGS. 1-9. A representative process flow for forming the cell stack shown in FIG. 10 is illustrated in FIG. 16. Representatively, process 1600 may include forming the first plurality of devices (e.g., compound semiconductor devices 302) on a first donor substrate (e.g., substrate 102) (block 1602). The first plurality of devices can then be attached to a receiving structure (e.g., structure 602) as previously discussed (block 1604). The receiving structure may include receiving devices which are aligned with the first plurality of devices. The first donor substrate can then be removed from the first plurality of devices as previously discussed to expose a surface of the first plurality of devices (block 1606). The second plurality of devices are formed on a second donor substrate (block 1608) and then attached to the exposed surface of the first plurality of devices (block 1610). The second plurality of devices can be attached to the first plurality of devices using the chemical and/or mechanical bonding steps previously discussed in reference to FIGS. 8-9. Once the first plurality of devices and the second plurality of devices are bonded together, the second donor substrate is removed (block 1612). Further processing may then be performed on the resulting device stack (e.g.,