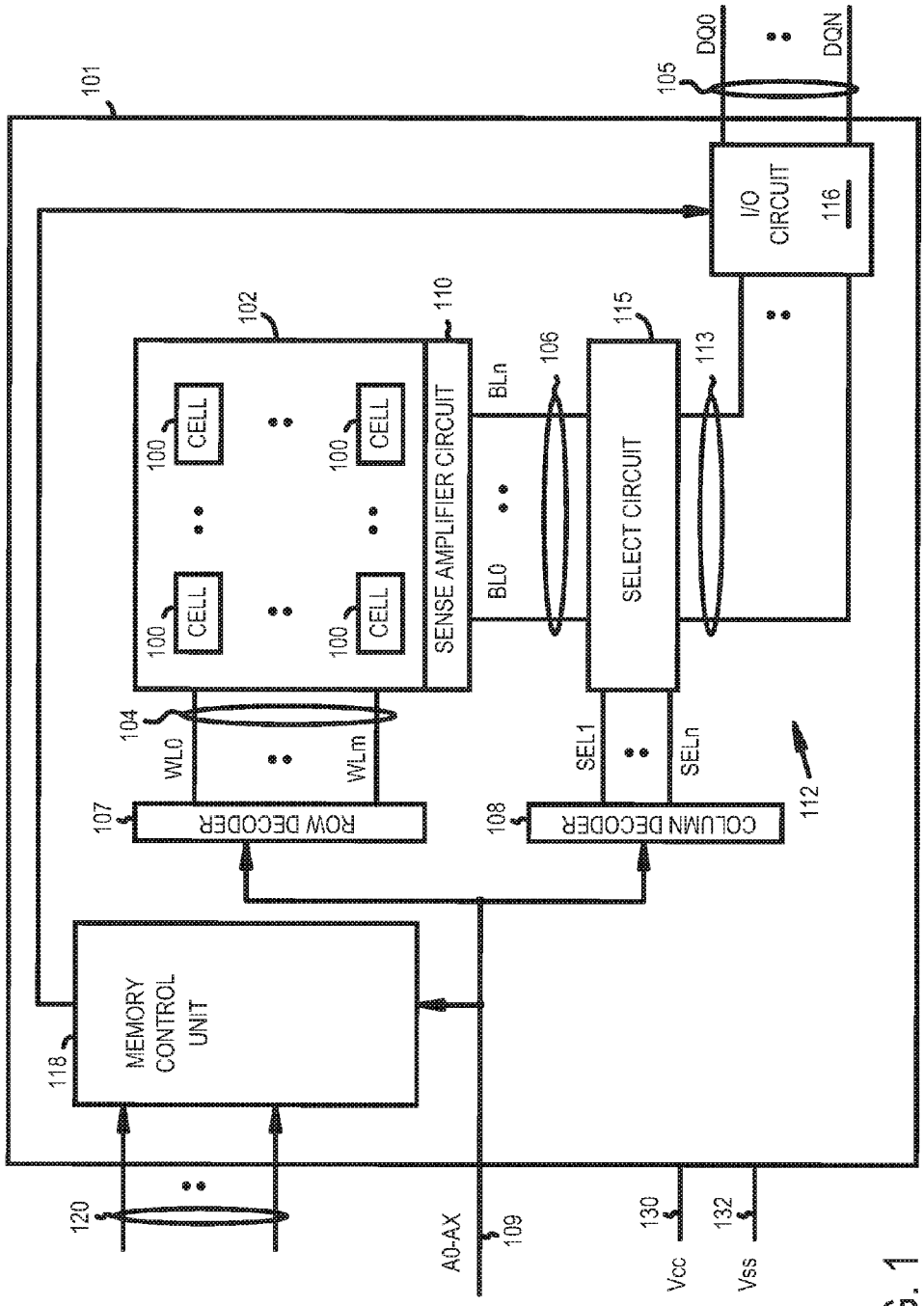
101
105
DQ0
DQN
I/O CIRCUIT
116
102
110
115
106
113
CELL
100
SENSE AMPLIFIER CIRCUIT
BLn
BL0
SELECT CIRCUIT
104
WL0
WLm
SEL1
SELn
112
107
ROW DECODER
108
COLUMN DECODER
MEMORY CONTROL UNIT
118
120
A0-AX
109
130
Vcc
132
Vss

FIG. 1