nents such as the communications transceiver noted above. Cache controller **222** may include a plurality of status bits including, without limitation, the following four status bits: RAM_fill_mode **224**, Cache_Enable **226**, DM/2SA **228** and Full_RAM_base **230** and local RAM/cache ("LR/C") **231**, as well as other bits that are not specifically shown in **FIG. 7**. The two-way associative cache may be configured as a direct map and its other way configured as a RAMset. Alternatively, the two-way set associative cache may be configured as two additional RAMsets depending on cache control bit DM/2SA **238** and FULL_RAM_Set_base **230** as described in at least one of the documents incorporated herein by reference. However, the preferred configuration comprises a single RAMset coupled to a standard data cache. The RAMset is not limited in size, nor must the RAMset have the same size as the other cache way. Therefore, if another RAMset is needed for capacity reasons, a single RAMset with a larger capacity may be preferred.

[**0048**] As shown, cache controller **222** couples to, or otherwise acceses, Full_Set_Tag registers **232** (individually referenced as registers **232***a* through **232***c*), Global_Valid bits **234** (individually referenced as bits **234***a* through **234***c*), tag memories 236 (individually referenced as tag memories **236***b* and **236***c*), valid entry bit arrays **237** (individually referenced as bit arrays **237***a* through **237***c*) and data arrays **238** (individually referenced as data arrays **238***a* through **238***c*). Comparators **240** (individually referenced as comparators **240***a* through **240***c*) may couple to respective Full_Set_Tag registers **232**. Comparators **242** (individually referenced as comparators **242***b* and **242***c*) couple to respective tag memories **236**. Output buffers **244** (individually referenced as buffers **244***a* through **244***c*) may couple to respective data arrays **238**. Hit/Miss logic **246** (individually referenced as logic **246***a* through **246***c*) may couple to comparators **240**, global valid bits **234**, valid bits **237**, RAM_fill_mode bit **224** and Cache_Enable bit **226**.

[**0049**] In operation, data storage **122** may be configured using the control bits **224**, **226**, **228** and **230**. The Cache_Enable **226** allows the data storage to be enabled or disabled, as in standard cache architecture. If the data storage **122** is disabled (e.g., Cache Enable=0), data read accesses may be performed on the main memory **106** without using the data storage **122**. If the data storage **122** is enabled (e.g., Cache_Enable=1), data may be accessed in the data storage **122**, in cases where such data is present in the data storage. If a miss occurs, a line (e.g., 16 bytes) may be fetched from main memory **106** and provided to the core **120**.

[**0050**] The size of the data array **238***a* may be different than the size of the data arrays **238***b, c* for the other ways of the cache. For illustration purposes and without limiting this disclosure in any way, it will be assumed that data arrays **238***b* and **238***c* are each 8 Kbytes in size, configured as 512 lines, with each line holding eight two-byte data values. Data array **238***a* may be 16 Kbytes in size, configured as 1024 lines, each line holding eight, two byte data values. The ADDR[L] signals may be used to address one line of the data array **238** and valid bit array **237** (and tag memory **236**, where applicable). Accordingly, for the 1024-line first way, ADDR[L] may include 10 bits [13:4] of an address from the core. For the 512-line second and third ways, ADDR[L] may include 9 bits [12:4] of an address from the core. The ADDR[H] signals define which set is mapped to a line. Thus, assuming a 4 Gbyte address space, ADDR[H] uses bits [31:14] of an address from the core for the first way and uses bits [31:13] for each of the second and third ways of the cache **130**.

[**0051**] The tag memories **236** and comparators **242** may be used for a two-way set associative cache (e.g., D-cache **124** in **FIG. 3**). When the core **120** performs a memory access, the tag memories **236** are accessed at the low order bits of the address (ADDR[L]). The tag memory locations store the high order address bits of the main memory address of the information stored in a corresponding line of the data array **238**. These high order address bits may be compared with the high order address bits (ADDR[H]) of the address from the core **120**. If the ADDR[H] matches the contents of the tag memory at ADDR[L], a hit occurs if the valid bit associated with the low order bits indicates that the cache entry is valid. If a cache hit occurs, the data from the corresponding data array **238** at ADDR[L] may be provided to the core **120** by enabling the corresponding output buffer **244**. As described below, data from the two-way cache is presented to the core **120** if there is a miss in the RAMset cache. By itself, the operation of the two-way set associative cache and the direct map cache may be conventional and may not be affected by the RAMset cache **126**. Other cache techniques could also be used in place of the two-way cache **124**.

[**0052**] The RAMset cache **126** preferably stores data associated with a contiguous block of main memory **106** starting at an address defined by the Full_set_tag register **232** for the RAMset. This contiguous block of information (e.g., local variables/pointers) may be mapped to the corresponding data array **238** of the RAMset. In at least some embodiments, only the high order bits of the starting address are stored in the Full_set_tag register **232**. **FIG. 8** illustrates this mapping for a single RAMset. As shown, the contents of Full_set_tag register **232***a* define the starting address for a contiguous block of memory cached in data array **238***a*.

[**0053**] Referring again to **FIG. 7**, a RAMset miss may occur when the high order bits of the address from the core **120** do not match the contents of the Full_set_TAG register **232** or the global valid bit is "0". In either case, when a RAMset miss occurs, the data storage **122** may behave like conventional, two-way cache logic. As such, if there is a hit in the two-way associative cache, then data is presented to the core **120** from the two-way set associative cache. Otherwise, the data is retrieved from main memory **106**, forwarded to the core and loaded into a "victim" entry of the two-way associative cache.

[**0054**] A RAMset hit situation may occur when the high order bits of the address from the core **120** match the contents of the Full_set_TAG register **232** and the global valid bit equals "1" (the setting of the global valid bit is described in greater detail below). By default, the RAMset comparison preferably has higher priority than the other cache ways. A hit situation indicates that the requested data is mapped into the RAMset. If the Valid entry bit **237** corresponding to the line containing the data is set to "1", comparator **240** causes hit/miss logic **246** to generate a "hit-hit" signal because the address hit the RAMset and the data is present in the RAMset. If the corresponding valid bit **237** of the RAMset entry is "0", logic **240** generates a "hit-miss" because the address hit the RAM set, but the data is not yet present in the RAM set. In this latter case, the data