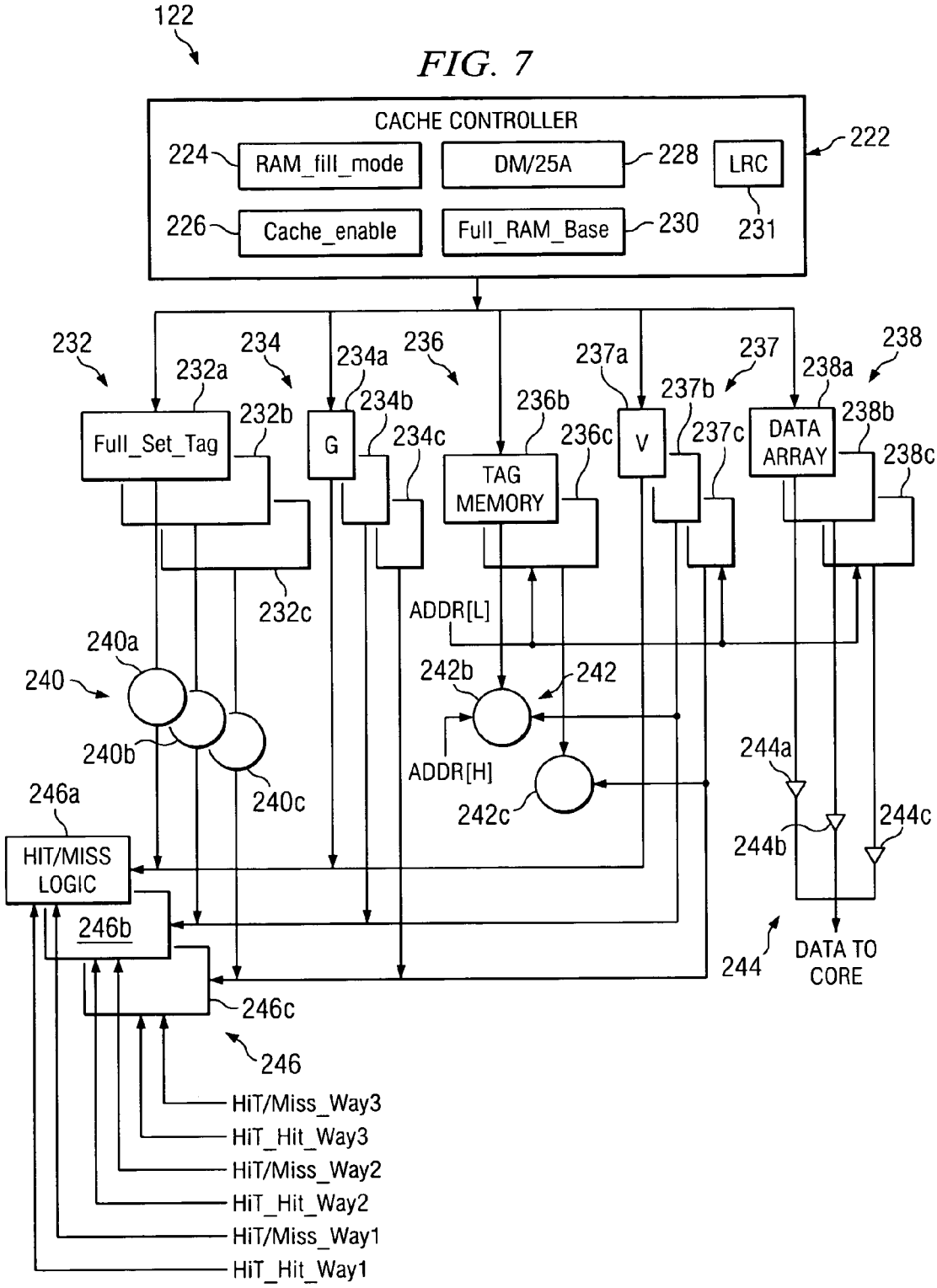
122
FIG. 7
CACHE CONTROLLER
224
RAM_fill_mode
DM/25A
228
LRC
222
226
Cache_enable
Full_RAM_Base
230
231
232
232a
234
234a
236
237a
237
238
238a
Full_Set_Tag
232b
G
234b
236b
V
237b
DATA ARRAY
238b
234c
236c
237c
TAG MEMORY
238c
232c
ADDR[L]
240a
240
242b
242
240b
ADDR[H]
244a
240c
242c
244c
246a
244b
HIT/MISS LOGIC
246b
244
DATA TO CORE
246c
246
HiT/Miss_Way3
HiT_Hit_Way3
HiT/Miss_Way2
HiT_Hit_Way2
HiT/Miss_Way1
HiT_Hit_Way1