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(54) SEMICONDUCTOR DEVICE

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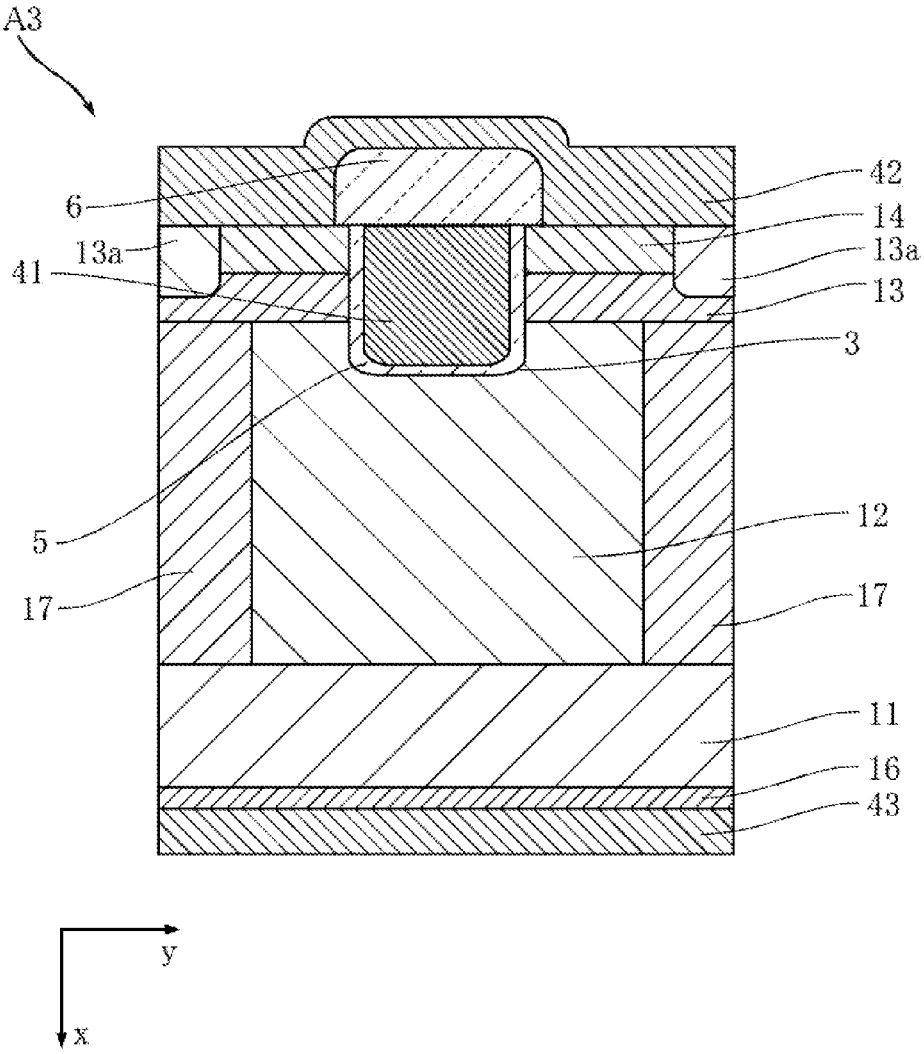
(57) **ABSTRACT**

A semiconductor device (**A1**) includes a first n-type semiconductor layer (**11**), a second n-type semiconductor layer (**12**), a p-type semiconductor layer (**13**), a trench (**3**), an insulating layer (**5**), a gate electrode (**41**), and an n-type semiconductor region (**14**). The p-type semiconductor layer (**13**) includes a channel region that is along the trench (**3**) and in contact with the second n-type semiconductor layer (**12**) and the n-type semiconductor region (**14**). The size of the channel region in the depth direction x is 0.1 to 0.5 μm. The channel region includes a high-concentration region where the peak impurity concentration is approximately 1×10^{18} cm^{-3}. The semiconductor device **A1** thus configured allows achieving desirable values of on-resistance, dielectric withstand voltage and threshold voltage.