

quencies of the ClkA and ClkB signals would each be determined over separate non-overlapping time intervals. The schematic diagram of **FIG. 3A** shows how signal diodes **D1**, **D2** may be used to disable (e.g., ground) the non-enabled oscillator by attenuation.

[0034] In an alternative embodiment, a single oscillator may be analog switched between the two conductive plates, yielding frequency differences primarily from the conductive plate capacitances rather than from variations in parts. An example of such an embodiment **150** is shown in **FIG. 1B**, wherein a switch **160** is used to connect either the first or second conductive plates **101**, **102** to the oscillator **103**.

[0035] In a further embodiment, the touch slider may utilize other methods for determining the capacitance of the capacitive nodes (and thus the finger position) by, e.g., generating signals whose amplitudes (instead of frequencies) are related to the capacitances of the capacitive nodes. In such a case, the ratio of the amplitudes may be used instead of the ratio of the frequencies or the pulse counts. In further embodiments, a charge transfer method may be employed to determine the respective capacitances of the individual capacitive nodes.

[0036] Referring to **FIG. 3A**, another exemplary capacitive touch slider **300** is shown. The circuit of **FIG. 3A** uses a processor such as an on-board PIC microprocessor **IC1**, wherein data is output via an interface port such as a 9600 baud serial port **350**. **FIG. 4** shows a timing diagram describing the relationship between various signals in the circuit of **FIG. 3A**.

[0037] The number of pulses of ClkA (the output of a first oscillator, which may preferably average about 2 MHz) is accumulated over a short interval (e.g., approximately 1 millisecond) while OscB is disabled. Immediately afterward, ClkB (the output of a second oscillator) is accumulated over another interval of the same length. Preferably, these two intervals are non-overlapping. The PIC microprocessor **IC1** then derives a finger position which is a function of the ratio of accumulated ClkA and ClkB pulses. A kind of "pressure" indication may also be derived and used to determine the threshold for finger contact from the sum of accumulated pulses of ClkA and ClkB.

[0038] A voltage regulator such as a 78L05 device **IC2** provides a regulated 5 volts for the circuit power. The PIC 16C73 CMOS microcontroller **IC1** provides control signals, data read and serial output for operation. Schmitt inverters for the two oscillators and for other portions of the circuit may be embodied in a 74HCT14 device **IC3**, which is a CMOS hex Schmitt inverter. A counter may also be used, such as a 74HC590 device **IC4**, which is a CMOS 8 bit counter with output latches, output tristate enable, and a counter clear. Since this embodiment measures capacitances on the order of a few picofarads, it is preferable that the RC oscillators (74HCT14) be disposed near the PC traces.

[0039] Referring to the timing diagram of **FIG. 4** in conjunction with the schematic diagram of **FIG. 3A**, during the count and read cycles, signal CapA/B* goes high to disable diode **D1**, thereby enabling RC oscillator **A** (comprising conductive plate **301**, resistor **R2**, and Schmitt inverter **IC3A**, which is one of the inverters in hex inverter device **IC3**). Raising CapA/B* to high also disables RC oscillator **B** (comprising conductive plate **302**, resistor **R3**,

and Schmitt inverter **IC3C**, which is also part of inverter device **IC3**) by grounding its input through diode **D2** using inverter **IC3F** (also one of the inverters of hex inverter device **IC3**). The CompClk signal reflects ClkA during this period. Next, the microprocessor **IC1** asserts En*Clr*, which is the clock enable and clear signal. **IC3D**, **IC3E**, **C7**, and **R7** together embody a falling edge pulse generator that provides a negative pulse (e.g., approximately 1 microsecond in length) to the Clr* pin of the counter **IC4** on the leading edge or beginning of the count cycle. Thus, the counter **IC4** starts counting from zero a few microseconds after the beginning of the count cycle. During this count period, the microprocessor **IC1** enables a counter read by asserting Read* and counts the positive transitions of the most significant bit (MSB) **D7**. This allows an extension of the number of bits of the counter **IC4**. After a predetermined duration (e.g., 1 millisecond where a PIC microprocessor is used), the count cycle is terminated by causing En*Clr* to go high. The 8 bits of the counter **IC4** are then read by the microprocessor **IC1**, combined with the number of low to high transitions of the MSB, and the result stored. CapA/B* is next negated to enable oscillator **B** (and also to ground oscillator **A**'s input or otherwise disable oscillator **A**) and the count cycle repeated, accumulating the total count of ClkB.

[0040] It is possible that external noise may be present on the power pins to the hex Schmitt inverter **IC1**, which may cause small uncompensated variations in the processed output. Filtering beyond the usual bypass capacitor may accordingly be required. A temporary RC filter may be added to the power input pin of the 74HCT14 to correct this problem. Also, where an additional control signal is derived from the local microprocessor, the counter clear pulse generator may be eliminated. As for critical timing, reading the counter's **D7** bit preferably should not begin until after more than 1 micro-second has passed after the leading edge of En*Clr* signal, due to the initial clearing of the counter with ClrPuls*. With an approximately 2.5 MHz clock frequency (for example) for oscillators **A** and **B**, the pulse accumulation may be approximately 2,500 (over a 1 millisecond period) and may provide an observed count range of approximately 150 on each accumulator within the normal finger position range.

[0041] Once the counts are accumulated and read by the microprocessor **IC1**, the microprocessor **IC1** may take a ratio of the counts, which entails either dividing the count of ClkA by the count of ClkB or vice versa. The microprocessor **IC1** may further add the two counts together and/or average them. Data representing the ratio and/or the sum/average may then be sent via the SerOut line to the interface **350**.

[0042] The count periods for both oscillators **A** and **B**, as well as the period between the count periods, may preferably be as short as possible to minimize any ambient 60 Hz interference (e.g., due to 60 Hz a-c power sources) that may be capacitively introduced through the finger. At 60 Hz, the period of the power source is $\frac{1}{60}$ second, or about 16.7 milliseconds. Accordingly, in one embodiment, the total count cycle for both oscillators **A** and **B** takes about 2.25 milliseconds, which is substantially less than 16.7 milliseconds. Thus, the power signal does not change substantially during the entire count period, thereby reducing the ambient noise caused by the power signal. If it is desired to update at 60 Hz, the overhead for controlling and reading the touch