

portion which extends above the plane of the pad or plate. When the electronics section is mated to the display section, the patterned material on the connecting plates **132** and connecting pads **142** come into contact and deform, providing an electrical connection between the corresponding connecting pads and plates. The pads **142** and plates **132** may also be connected by bump-bonding techniques or using wires that are implanted in one of the pads **142** or plates **132** and engage the plate **132** or pad **142** when the electronics section **104** is mated to its corresponding display section **102**.

[0052] Alternatively, the connecting plates **132**, connecting pads **142** and insulating layer **130** may be omitted and connection between the vias **144** and the row and column electrodes may be made by providing raised conductive bumps (not shown) on each of the vias **144** which are positioned to mate with corresponding raised conductive bumps (not shown) on the row and column electrodes of the display section **102**.

[0053] In any of these configurations, the display section may be joined to the electronics section using a non-conductive adhesive, if the respective bumps come into direct contact, or by an anisotropic conductive adhesive. The exemplary anisotropic conductive adhesive may be formed, for example by suspending particles of a conductive material in an adhesive such that, the particles touch and form conductive paths when pressure is applied to the adhesive. Alternatively, the particles may be formed from a ferromagnetic material and may be aligned in a desired conductive direction (e.g. vertically) using an externally applied magnetic field. Further details of this sealing and connecting method are described below with reference to **FIG. 20**.

[0054] As described above with reference to **FIG. 1**, the contrast of the display device in **FIG. 2** may be enhanced by adding a dark pigment to the adhesive which joins the electronics section **104** to the display section **102** or by using a clear or translucent adhesive and forming the circuit board **144** from a dark material to provide a dark background for the emissive materials **124** and **126**. To provide the most contrast enhancement, it is desirable for the contact pads **142**, contact plates **132** and insulating layer **130** to be omitted or, if present, to be transparent or translucent. Translucent pads **142** and plates **132** may be achieved by depositing these layers using thin-film techniques. In addition, as set forth above with reference to **FIG. 1**, it is desirable for the row electrodes to be masked from view by a dark-colored material or be formed from a transparent material.

[0055] The display structures shown in **FIGS. 1 and 2** may be used in a full-size display device or in a smaller tile. Many of the smaller tiles may be joined together to form a very large display device. **FIG. 3** is a bottom plan view of a display tile having the structure shown in **FIG. 1**. As shown in **FIG. 3**, the circuit board **120** includes electronic circuitry **134** which is connected to the rows and columns of the display through the vias **114** and **112** respectively. In the exemplary embodiment of the invention, the circuit board **120** may be formed from ceramic green tape which is punched or drilled to form holes for the vias **112** and **114**. The conductors **140** which connect the circuitry **134** to the vias **112** and **114** may be printed or painted onto the green tape and the via holes may be filled prior to firing. The

conductive traces **140** are coupled to the vias **112** and **114** along the edge of the circuitry **134**. The circuitry **134** is coupled to receive operational power via conductors **310** and to receive the data signal and timing information via conductors **312** and a connector **314**.

[0056] **FIG. 4** is a bottom plan view of a display tile having the structure shown in **FIG. 2**. This tile also includes electronic circuitry **134**, conductive traces **140** operational power conductors **310**, data and timing signal conductors **312** and connector **314**. The conductive traces **140** in this embodiment of the invention, however, are not limited to the edges of the tile but are connected to the row and column electrodes of the display device through interior pixel positions of the tile.

[0057] **FIG. 5** is a pixel diagram which illustrates an exemplary pixel spacing that may be used in the tile having the structure shown in **FIG. 1**. The routing of the vias **112** and **114** along the edges of the tiles allows multiple tiles to be abutted in a way which renders the joint between the tiles virtually invisible. The pixel spacing shown in **FIG. 5** allows the conductive vias to be arranged along the edge of the tile, without interrupting the continuity of the pixel spacing in the assembled tiled display. **FIG. 5** illustrates portions of four tiles, **530**, **540**, **550**, and **560**. The dashed lines **524** and **522** illustrate pixel boundaries. These lines are provided only as a guide in understanding the pixel layout. The active portion **526** of the pixels occupies only about $\frac{1}{4}$ of the total pixel area. This defines a pixel aperture of approximately 25%. The aperture is the ratio of the active pixel area to the inactive pixel area. In this exemplary embodiment of the invention, the active region is not centered in the pixel area but is offset to the left and top as shown in **FIG. 5**.

[0058] As shown in **FIG. 5**, this spacing of the pixels leaves room along the edges of the display for the vias **114** and **112** to connect to the row and column electrodes of the pixel without interfering with the regular spacing of the pixels across tile boundaries. In the exemplary embodiment shown in **FIG. 5**, the distance d_e , which is the distance from the active region **526** to the edge of the tile, is approximately twice the distance d_r which is the internal distance from the edge of the active area of the pixel **526** to the pixel boundary **112** or **114**.

[0059] Although the pixel diagram shown in **FIG. 5** has the active region of the pixel being offset both horizontally and vertically, it is contemplated that the active area may be offset only vertically. In this configuration, the contacts to the row electrodes are beneath the active pixel material and, thus, do not need to offset the active region of the pixel.

[0060] **FIG. 6** is an alternative pixel layout, suitable for use for a tile such as that shown in **FIG. 2**. In the layout shown in **FIG. 6**, the active portions **526** of the pixels are centered in their respective pixel regions and the vias **144** which connect the row and column electrodes of the display to the electronics are formed between respective pixel elements. The distance between the edge of an active region **526** and the edge **612** of the display is equal on all sides of the tile and the distance from the center of the active pixel region to the edge is $\frac{1}{2}$ of the pixel pitch. As described below with reference to **FIGS. 12 and 12A**, however, the distance between the center of an edge pixel and the edge of the tile may be slightly less than $\frac{1}{2}$ of the pixel pitch in order to allow a mullion to be inserted and join adjacent tiles. As