

[0055] Master transceiver 12 and slave transceivers 14a through 14n of the network 10 are structured and configured as transceiver device 22 as described herein. The transceiver node device 22 comprises an integrated circuit or like hardware device providing the functions described below. Transceiver device 22 comprises an antenna 24, a transmitter 26 connected to the antenna 24, a data modulation unit 28 connected to the transmitter 26, and an interface to Data Link Layer (DLL) 30 connected to the data modulation unit 28. The transceiver device 22 also includes a receiver 32 connected to the antenna 24 and a data demodulation unit 34 connected to the receiver 32 and to the interface to the interface to Data Link Layer (DLL) 30. A receive gain control unit 36a is connected to the receiver 32, a transmit gain control unit 36b is connected to the transmitter 26. A framing control unit 38 is operatively coupled to the data modulation unit 28 and the data de-modulation unit 34. A clock synchronization unit 40 is also operatively coupled to the data modulation unit 28 and the data demodulation unit 34.

[0056] Antenna 24 comprises a radio-frequency (RF) transducer as is known in the art and is preferably structured and configured as a receiving antenna and/or a transmitting antenna. As a receiving antenna, antenna 24 converts an electromagnetic (EM) field to an electric current, and as a transmitting antenna, converts an electric current to an EM field. In the preferred embodiment, antenna 24 is structured and configured as a ground plane antenna having an edge with a notch or cutout portion operating at a broad spectrum frequency ranging from about 2.5 gigahertz (GHz) to about 5 GHz with the center frequency at about 3.75 GHz. It will be appreciated that antenna 24 may be provided with various geometric structures in order to accommodate various frequency spectrum ranges.

[0057] Transceiver node device 22 includes hardware or circuitry which provides an interface to data link layer 30. The interface to data link layer 30 provides an interface or communication exchange layer between the Physical layer 22 and the "higher" layers according to the OSI reference model. The layer immediately "above" the Physical layer is the data link layer. Output information which is transmitted from the data link layer to the interface 30 is communicated to the data modulation unit 28 for further data processing. Conversely, input data from the data-demodulation unit 34 is communicated to the interface 30, which then transfers the data to the data link layer.

[0058] Transceiver node device 22 includes hardware or circuitry providing data modulation functions shown generally as data modulation unit 28. The data modulation unit 28 carries out the operation of converting data received from the interface 30 into an output stream of pulses. In the case of pulse amplitude modulation, the amplitude of the pulse represents a value for that symbol. The number of bits represented by a pulse depends on the dynamic range and the signal to noise ratio. The simplest case comprises on-off keying, where the presence of a pulse of any amplitude represents a "1", and the absence of a pulse represents "0". In this case, data modulation unit 28 causes a pulse to be transmitted at the appropriate bit time to represent a "1" or no pulse to be transmitted at the appropriate time to represent a "0". As described further below, the pulse stream produced by transceiver 22 must be synchronous with a master clock of the network 10 and must be sent at the

appropriate time slot according to a frame definition defined for the network. The pulse stream is then communicated to transmitter 26 for transmission via antenna 24.

[0059] Transceiver node device 22 includes hardware or circuitry providing means for transmitting data to other transceivers on the network shown generally as transmitter 26. The transmitting means of transceiver 22 preferably comprises a wide band transmitter 26. Transmitter 26 is operatively coupled to the data modulation unit 28 and to the antenna 24. Transmitter 26 carries out the operation of transmitting the pulse stream received from modulation unit 28 and transmitting the pulse stream as electromagnetic pulses via antenna 24. In the preferred embodiment, information is transmitted via impulses having 100 picosecond (ps) risetime and 200 ps width, which corresponds to the 2.5 through 5 GHz bandwidth.

[0060] Transceiver node device 22 includes hardware or circuitry which provides means for receiving data from other transceivers shown generally as receiver 32. The receiving means of transmitter 22 preferably comprises a wide band receiver 32. Receiver 32 is operatively coupled to the antenna 24 and the data demodulation unit 34. Receiver 32 carries out the operation of detecting electromagnetic pulse signals from antenna 24 and communicating the pulse stream to the data de-modulation unit 34. The received signal does not necessarily have the same spectrum content as the transmitted signal, and the spectrum content for received and transmitted signals vary according to the receive and transmit antenna impulse response. Typically, the received signal is shifted toward a lower frequency than the transmitted signal.

[0061] Transceiver node device 22 further includes hardware or circuitry providing means for controlling the gain of signals received and transmitted shown generally as gain control units 36a, 36b. The transmit gain control unit 36b carries out the operation of controlling the power output of the transmitter 26 and receive gain control unit 36a carries out the operation of controlling the input gain of the receiver 32.

[0062] As indicated above, the pulse stream produced by modulator 28 must be synchronous with the master clock of the network 10. In order to maintain a synchronized network, one device must serve the function of being a clock master and maintain the master clock for the network. Preferably, the master device 12 carries out the operation of the clock master. All other slave devices must synchronize with the master clock. The invention includes means for synchronizing the network system 10 provided by the clock synchronization unit 40 in transceiver 22.

[0063] Referring to FIG. 3a as well as FIG. 1 and FIG. 2, a functional block diagram of a clock synchronization unit 40a for the master device 12 is shown. In the master device 12, the clock synchronization unit 40a includes hardware or circuitry providing the functions described herein. Clock synchronization unit 40a comprises a clock master function 42 which maintains a master clock 44 for the network 10. The master clock 44 runs at a multiple of the bit rate. As described in further detail below, transmit time is divided into "frames", and transceiver devices are assigned specific "slots" within each frame where the devices are permitted to transmit data. At least once per frame, the clock master function 42 issues a master sync code. The master sync code