

is a unique bit pattern that does not appear anywhere else in the frame which identifies the sender as the master device 12.

[0064] Referring to FIG. 3b as well as FIG. 1 and FIG. 2, a functional block diagram of a clock synchronization unit 40b for the slave devices 14a through 14n is shown. In the slave devices 14a through 14n, the clock synchronization unit 40b includes hardware or circuitry providing the functions described herein. Clock synchronization unit 40b comprises a local or slave clock 46 and a clock recovery function 48. The slave clock 46 also runs at a multiple of the bit rate.

[0065] The clock recovery function 48 carries out the operation of scanning the incoming data stream received by receiver 32 to detect or otherwise ascertain the master sync code using one or more correlators. When the clock recovery function 48 detects the master sync code, the clock recovery function 48 will predict when the next master sync code will be transmitted. If the new master sync code is detected where predicted, the transceiver 22 will be considered "locked" or otherwise synchronized with the clock master 42 and will continue to monitor and verify future incoming master sync codes. If the clock recovery function 48 fails to detect a threshold number of consecutive master sync codes, lock will be considered lost. As each master sync code is received by the transceiver, a phase or delayed locked loop mechanism is used to adjust the phase of the slave clock 46 to that of the incoming pulse stream.

[0066] The clock recovery function 48 includes a master sync code correlator 50. A slave transceiver trying to achieve synchronization or "lock" with the master clock examines the incoming data stream to detect the master sync code, as described above. The master sync code correlator 50 carries out the operation of detecting the first incoming pulse and attempting to match each of the next arriving pulses to the next predicted or pre-computed pulse. After the initial master sync code is detected, the clock recovery function 48 of the slave transceiver device will perform a coarse phase adjustment of its bit-clock to be close to that of the incoming pulse stream. When the next master sync code is expected, a mask signal is used to examine the incoming pulse train stream only where valid pulses of the incoming master sync code are expected. The primary edge of the incoming pulse is compared with the rising edge of the local clock, and any difference in phase is adjusted using a phase-locked loop mechanism. If the incoming pulse stream matches the master sync code searched for, the correlator 50 signals a successful match. If the incoming pulse stream differs from the master sync code, the process is repeated. Multiple correlators may be used to perform staggered parallel searches in order to speed up the detection of the master sync code.

[0067] The clock recovery function 48 further includes a phase lock mechanism 52. As each predicted master sync code is detected at the slave transceivers, the phase lock mechanism 52 carries out the operation of determining the phase difference between the local slave clock 46 and the incoming pulses. The phase lock mechanism 52 adjusts the phase of the slave clock 46 so that the frequency and phase of the slave clock 46 is the same as that of the incoming pulses, thereby locking or synchronizing the local slave clock 46 to master clock 44 of the master transceiver 12.

[0068] Referring again to FIG. 2, as well as FIG. 1, the transceiver node device 22 includes hardware or circuitry

which provides demodulating functions and is shown generally as data demodulation unit 34. The data demodulation unit 34 carries out the operation of converting the input pulse stream from receiver 32 into a data stream for higher protocol layers. The data de-modulation unit 34 comprises a phase offset detector 54 and a data recovery unit 56. In an isochronous baseband wireless network, data streams will be received from different transceivers with different phase offsets. The phase offset is due to path propagation delays between the transmitter, the receiver and the master clock 44.

[0069] As described in further detail below, a transmitter will be assigned a data "slot" within a frame to transmit to another device. The phase offset detector 54 carries out the operation of ascertaining the phase delay between the expected zero-delay pulse location, and the actual position of the incoming pulses. Typically, a known training bit pattern is transmitted before the data is transmitted. The phase offset detector 54 in the receiving device detects or otherwise ascertains the training bit pattern and determines the phase offset of the incoming pulse from the internal clock. The phase determined is then communicated to the Data Recovery Unit 56. In the case of pulse amplitude modulation, the training sequence is also used to provide a known pulse amplitude sequence against which the modulated pulse amplitudes can be compared in the data transmission.

[0070] The Data Recovery Unit 56 in a receiving device carries out the operation of converting the incoming pulse stream data into bit data during time slots that a transmitting device is sending data to the receiving device. In the case of on-off keying modulation, the data recovery unit 56 carries out the operation of examining the pulse stream during the designated time slot or "window" for the presence or absence of a pulse. In pulse amplitude modulation, the data recovery unit 56 carries out the operation of examining the pulse stream during the designated time slot or "window" to ascertain the amplitude of the pulse signal. The "window" or time slot in which the receiving device examines pulse stream data determined by the expected location of the bit due to the encoding mechanism and the offset determined by the phase offset detector 54. The information converted by the data de-modulation unit 34 is then communicated to the interface to data link layer 30 for further processing.

[0071] Referring now to FIG. 4 as well as FIG. 1 and FIG. 2, a Time Division Multiple Access (TDMA) frame definition is shown and generally designated as 58. The TDMA frame definition 58 is provided and defined by the data link protocol software of the present invention. More particularly, the TDMA frame 58 is defined by the Medium Access Control (MAC) sublayer software residing within the Data Link Layer according to the OSI Reference model.

[0072] The means for managing the data transmission between the transceiver nodes of the network 10 is provided by software algorithms running and executing in the Medium Access Control. The Medium Access Control protocol provides algorithms, routines and other program means for managing and controlling access to the TDMA frame definition 58 and its associated slot components. The architecture of TDMA frame definition 58 provides for isochronous data communication between the transceivers 12, 14a through 14n of the network 10 by providing a means