

4B/5B or similar encoding scheme and provides the resulting bit stream to the Mux/Demux unit **74** via line **86a**. The data to be transmitted is provided through the interface **73** via line **85a**. The input buffer unit **80** receives data from the Physical layer through the Mux/Demux unit **74** via line **86b**, decodes it according the same 4B/5B or similar encoding scheme, and stores the data in a FIFO buffer (not shown) which is connected to the data path interface **73** via line **85b**. Lines **85a** and **85b** are operatively coupled to data interfaces **76a** through **76n** for communication with interface **73**. Lines **86a** and **86b** are operatively coupled for communication with Mux/Demux unit **74**.

[0098] The control logic unit **82** comprises a state machine that controls the operation of the output buffer unit **78** and input buffer unit **80** as well as the communication between the MAC and the Logical Link Layer (LLC), and the MAC and the Physical Layer. The values of the control registers **84** are set by the LLC above the MAC layer via line **88** and control the operation of the SAU.

[0099] The control registers **84** comprise a SAU enable register **90**, a data transfer direction register **92**, a slot start time register **94**, and a slot length register **96**. The SAU enable register **90** determines whether the SAU **72** should transmit or receive data. The data transfer direction register **92** determines whether the SAU **72** is set up to transmit to the Physical Layer or to receive from the Physical Layer. The slot start time register **94** provides the SAU **72** with the time offset of the slot measured from the start of the frame, during which the SAU **72** transmits data to the Physical Layer.

[0100] The slot length register **96** determines the length of the slot. The status registers **84** provide the LLC with information about the current state of the SAU. The status registers comprise an input buffer unit empty flag, an input buffer unit full flag, an output buffer unit empty flag, an output buffer unit full flag, and an input decoder error counter. The buffer unit empty flag indicate whether the respective buffer units are empty (i.e., contain no data). The buffer unit full flag indicate whether the respective buffer units are full (i.e., cannot store additional data). The input decoder error counter indicates the number of error detected during the decoding of data arriving from the Physical Layer.

[0101] The SAU **72** transmits or receives data autonomously after being set up by the LLC. The setup consists of writing appropriate values into the data transfer direction register **92**, the slot start time register **94**, and the slot length register **96** and then enabling the SAU **72** by asserting the SAU enable register **90**. The slot start time and slot length values provided in registers **94**, **96** respectively are designated to the communicating device by the network master **12**. These values are determined by the master **12** in such a way that no two transmitters in the network transmit at the same time, a requirement of the TDMA communication scheme. During transmission, the SAU **72** will monitor the current time offset within the frame and compare it with the slot start time. When the two values are equal, the SAU **72** will provide the Physical Layer with encoded data bits from the output buffer **78** until the frame has reached the end of the time slot allocated to the SAU **72** as determined by the slot length register **96**. If the output FIFO buffer is empty

during the allocated time slot, the SAU **72** will transmit special bit codes indicating to the receiver that there is no data being transmitted.

[0102] Likewise, the SAU **72** will monitor the current time offset within the frame during data reception and compare it to the slot start time register **94**. When the two values are equal, the SAU **72** will acquire data from the Physical Layer through the Mux/Demux Unit **74**, decode it and store the decoded data in the input FIFO buffer. If the decoder detects a transmission error, such as a bit code sequence not found in the 4B/5B encoding table, the data stored in the input FIFO buffer is marked as invalid and the input decoder error counter is incremented. If the decoder detects special bit codes indicating empty data, the latter are ignored and will not be stored in the input FIFO buffer.

[0103] Accordingly, it will be seen that this invention provides a wireless communication network system for isochronous data transfer between node devices of the network, which provides a master node device having means for managing the data transmission between the other node devices of the network system, which further provides means for framing data transmission and means for synchronizing the network communication protocol, thus providing a means for sharing the transport medium between the node devices of the network so that each node device has a designated transmit time slot for communicating data. Although the description above contains many specificities, these should not be construed as limiting the scope of the invention but as merely providing an illustration of the presently preferred embodiment of the invention. Thus the scope of this invention should be determined by the appended claims and their legal equivalents.

What is claimed is:

1. A wireless communication network system comprising at least three transceivers, each said transceiver having a transmitter and a receiver, one of said transceivers being structured and configured as a master device, said master device structured and configured to manage data transmission between said transceivers.

2. The wireless communication network system as recited in claim 1, wherein said transceivers operate according to a Medium Access Control protocol having a time division multiple access frame definition, said protocol structured and configured to operate in aloha mode and time division multiple access mode.

3. The wireless communication network system as recited in claim 1, wherein each said transceiver further comprises a framing controller, said framing controller having means for generating and maintaining time frame information for said network system.

4. The wireless communication network system as recited in claim 1, further comprising a frame definition having a master slot, a command slot, and a plurality of data slots, said master slot having a master sync code, said protocol operating in slotted aloha mode and time division multiple access mode, said master device managing said protocol and said data slots in said protocol.

5. The wireless communication network system as recited in claim 1, further comprising a Medium Access Control hardware interface comprising a multiplexer/demultiplexer unit and a plurality of slot allocation units, said multiplexer/demultiplexer unit operatively coupled to said plurality of slot allocation units.