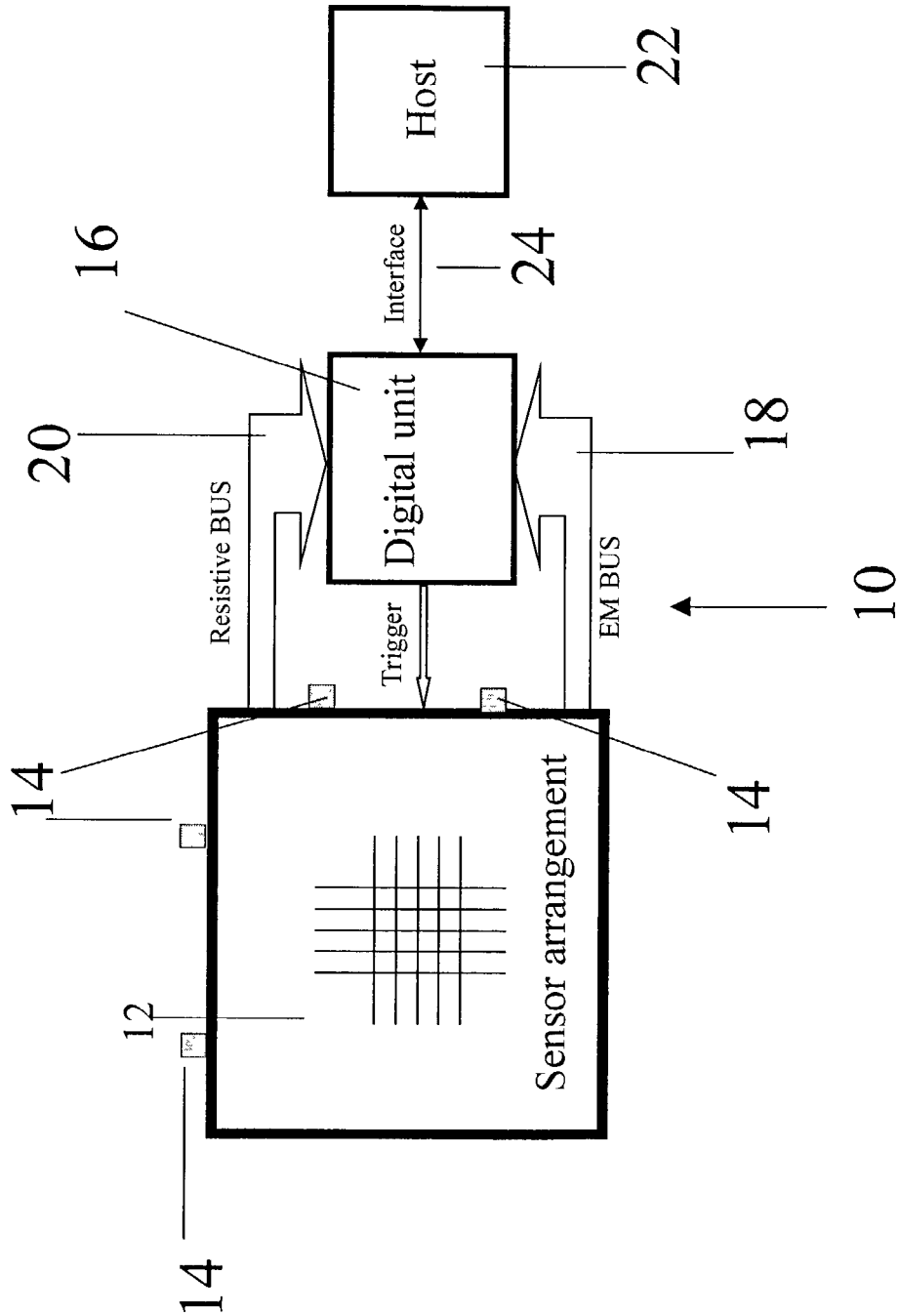
Fig. 1


Host
22
Interface
24
16
Digital unit
20
18
Resistive BUS
EM BUS
Trigger
10
14
14
Sensor arrangement
12
14