

through the microcoil and the inductance of the microcoil; the inductance of the microcoil is in turn proportional to the number of turns of the microcoil and the size (diameter) of the microcoil. Accordingly, a microcoil design that provides a relatively high inductance generally is desirable to provide for a magnetic field of sufficient strength to trap samples. At the same time, to maintain a fine spatial resolution amongst the microcoils of the array and facilitate sample transport between adjacent microcoils, it is generally desirable to have a relatively small inter-coil spacing or pitch **216** and relatively small diameter **214** of the upper portion **212A** of a microcoil, as indicated in FIG. 6(a).

[0109] Accordingly, in various aspects of this embodiment, the overall number of turns of the microcoil and the diameter of each coiled portion is appropriately selected to provide an appropriate array pitch, as well as an appropriate microcoil inductance to generate sufficient magnetic fields, to facilitate sample trapping and transport between microcoils. To this end, the multiple layer microcoil structure shown in FIGS. 7 and 8 uses vertical space in the layered CMOS chip design to obtain a greater number of turns per microcoil to provide for higher inductance. At the same time, distributing the turns amongst different levels or portions of the microcoil allows for different diameters in different levels/portions of the microcoil, which facilitates small inter-coil spacing or pitch between adjacent coils while at the same time providing an effective microcoil inductance.

[0110] More specifically, in the exemplary microcoil shown in FIGS. 7 and 8, the upper portion **212A**, which is closest to the surface of the IC chip—and hence closest to samples in the microfluidic chamber, may be fabricated as a single turn of a metal conductor having a relatively small diameter **214**, the size of which may be determined by the average size of a sample that is to be trapped. In one exemplary implementation, the diameter **214** of the upper portion **212A** may be on the order of approximately 10-11  $\mu\text{m}$ ; it should be appreciated that generally this diameter is greater than approximately 5  $\mu\text{m}$ , due to present limitations of CMOS fabrication techniques. The diameter **214** of the upper portion **212A** also may be selected, based at least in part, on the overall desired size of the microcoil array **200B** and the desired pitch **216**. In general, to ensure appropriate resolution between adjacent magnetic fields, the spacing between upper portions of adjacent microcoils should be no less than approximately the diameter **214** of each of the upper portions; this results in a pitch **216** approximately twice that of the diameter **214** (again, it should be appreciated that increased resolution of the array is fundamentally limited by the resolution of the fabrication process). Based on this general relationship, in various implementations, the diameter **214** and the pitch **216** can range from a couple of micrometers to a few tens of micrometers, depending on types of samples under consideration and applications involved.

[0111] As also illustrated in FIGS. 7(a) and (b), the middle portion **212B** and the lower portion **212C** of the microcoil may have larger diameters than the upper portion. In one aspect, the larger diameters of the middle and lower portions is possible because the spacing between adjacent middle and lower portions of adjacent microcoils in the array may be smaller than the spacing between adjacent upper portions without compromising the resolution of the generated mag-

netic fields (i.e., the resolution of the generated magnetic fields is largely determined by the top metal layer). Thus, the middle and lower portions generally may include a greater number of turns and/or a larger diameter than the upper portion, thereby providing for a relatively higher microcoil inductance. Additionally, as shown in FIGS. 7(a) and (b), the lower portion **212C** may include tabs **228** to facilitate connection of the microcoil **212** to a current (or voltage) source, as discussed further below. In one exemplary implementation, each of the middle and lower portions may include three conductor turns, wherein a diameter **220** of the middle portion **212B** may be on the order of approximately 20-25  $\mu\text{m}$ , and a diameter **218** of the lower portion **212C** may be on the order of approximately 15-20  $\mu\text{m}$  (the relatively smaller diameter of the lower portion permits the inclusion of the tabs **228**). In other implementations, different numbers of conductor turns and/or different dimensions may be used for respective coil portions, and may be determined empirically or based on numeric simulations of desired magnetic fields for different applications.

[0112] With reference now to the IC vertical layer structure illustrated in FIG. 8, the IC chip **102** includes a semiconductor substrate layer **104**, above which is sequentially fabricated the three layers/portions **212C**, **212B** and **212A** of the microcoil **212**. Each of the layers/portions **212C**, **212B** and **212A** may be formed by deposition and patterning of a conducting metal, such as copper, gold, or aluminum, for example. The multiple metal layers are separated from each other and other layers of the IC chip by an insulating material **112** comprising, for example, silicon oxide ( $\text{SiO}_2$ ) or another suitable dielectric material. The three layers/portions **212C**, **212B** and **212A** are electrically coupled together to create a continuous multi-layer conducting loop by vias **114** (e.g., made of tungsten) that extend through the insulating material **112** (the vias **114** also are indicated in the perspective view of FIG. 7(a)).

[0113] In one embodiment, the CMOS processing techniques employed to fabricate the vertical layer structure shown in FIG. 8 (e.g., Taiwan Semiconductor Manufacturing Company CMOS 0.18  $\mu\text{m}$  technology) yield a thickness **222** for the upper metal layer/portion **212A** of approximately 1 to 3  $\mu\text{m}$ . The upper metal layer also may be patterned such that the line width in the x-y plane (i.e., perpendicular to the plane of FIG. 8) of the metal conductor is also approximately 1 to 3  $\mu\text{m}$ , such that the metal conductor cross section for the upper portion **212A** is from approximately  $1 \times 1 \mu\text{m}^2$  to approximately  $3 \times 3 \mu\text{m}^2$  (it should be appreciated that, based on the TSMC 0.18  $\mu\text{m}$  design rule, the line width of the upper metal layer—metal **6**—may be as small as 0.44  $\mu\text{m}$ ).

[0114] With respect to the middle and lower layers/portions **212B** and **212C**, the CMOS processing techniques may yield a thickness **224** for both the lower and middle layers/portions of approximately 0.5 to 1  $\mu\text{m}$ . These layers may be patterned such that the line width in the x-y plane is also approximately 0.5 to 1  $\mu\text{m}$ , yielding a metal conductor cross section for the lower and middle portions of approximately  $0.5 \times 0.5 \mu\text{m}^2$  to approximately  $1 \times 1 \mu\text{m}^2$ . A distance **226** between the metal layers may be on the order of approximately 1  $\mu\text{m}$  (it should be appreciated that, based on the TSMC 0.18  $\mu\text{m}$  design rule, the distance between the metal layers may be as small as 0.46  $\mu\text{m}$ ).