

equations (4) and (5), a “lock frequency” ω_{lock} for the frequency locked loop may be expressed as

$$\omega_{\text{lock}} = \sqrt{\left(\frac{1}{LC_{\text{RF}}}\right)\left(\frac{R_1 + R_L}{R_2 + R_C}\right)}. \quad (6)$$

[0158] From the foregoing, it may be appreciated that the lock frequency ω_{lock} is essentially a function of changes in the microcoil inductance L, as C_{RF} , R_L , R_C , R_1 , and R_2 , are known fixed values. In one exemplary implementation, a nominal microcoil inductance L on the order of 1 nH is considered, with a nominal coil resistance R_L of approximately 50 Ω . To ensure that ω_{lock} is below or approximately 100 MHz, C_{RF} is chosen at 1 pF, with a typical R_C on the order of approximately 1 k Ω , R_1 is chosen at approximately 50 Ω and R_2 is chosen at approximately 10 k Ω .

[0159] To measure changes in inductance ΔL due to the presence of a magnetic sample in proximity to a microcoil, an instantaneous lock frequency ω_{lock} is measured and compared to a nominal lock frequency representing the absence of a magnetic sample. In exemplary implementations in which ω_{lock} is nominally approximately 100 MHz in the absence of a magnetic sample, changes in the lock frequency $\Delta\omega_{\text{lock}}$ due to the presence of a magnetic sample may be on the order of approximately 50 to 100 kHz. In FIG. 17, the buffer amplifier 488 is employed to transform $V(\omega)$ to a square wave, for which an edge counter 490 may be employed (e.g., a series of flip-flops) to determine changes in the frequency ω . In particular, in one implementation, the edge counter 490 may be configured to count square wave edges during a given time period and provide a digital output representing such a count to the one or more processors 600 shown in FIGS. 1 and 2, from which changes in the frequency ω representing the presence of a sample may be determined.

[0160] In the circuit arrangement illustrated in FIG. 17, the function of the phase detector 482 is to output a current $I=K_{\theta}(\theta_2-\theta_1)$, where K_{θ} is some constant. This current I is applied to the low pass filter 484 which, in the Laplace domain, has a transfer function

$$Z(s) = \frac{s+z}{s(s+p)}, \quad (7)$$

where z is a zero and p is a pole of the transfer function. From the foregoing, it can be seen that the transfer function Z(s) includes a pole at $s=0$ in the denominator, due to the presence of the capacitor 484A. An expression for the control voltage V_C in the Laplace domain then may be given as

$$V_C(s)=IZ(s)=K_{\theta}(\theta_2-\theta_1)Z(s). \quad (8)$$

From the foregoing, it may be observed that in steady state ($s=0$), Z(s) tends to infinity; hence, to ensure a stable control voltage V_C , the quantity $(\theta_2-\theta_1)$ must tend to zero in steady state. Accordingly, the capacitor 484A in the low pass filter 484 essentially ensures that the frequency locked loop stabilizes when $\theta_2=\theta_1$, thereby providing the expression for ω_{lock} given above.

[0161] FIG. 18 illustrates further details of the phase detector 482 of the frequency locked loop shown in FIG. 17, according to one embodiment of the present disclosure. As shown in FIG. 18, the phase detector includes two phase comparators 4821 and 4822, each designed to output an “up” signal or a “down” signal based on a phase relationship between the two signals applied to the comparator. For example, taking the signal $V(\omega)$ as a reference signal applied to each comparator, a given comparator outputs a pulse width modulated “up” signal if the other input signal to the comparator leads the reference signal; alternatively, the comparator outputs a pulse width modulated “down” signal if the other input signal lags the reference signal. A duty cycle of the respective up and down signals is proportional to the amount of the corresponding lead or lag.

[0162] Based on the configuration of the bridge circuit 485 shown in FIG. 17, it may be observed that, in the phase detector 482 shown in FIG. 18, the signal $V_2(\omega)$ always leads the reference signal $V(\omega)$ by the phase θ_2 and the signal $V_1(\omega)$ always lags the reference signal $V(\omega)$ by the phase θ_1 . Accordingly, in the implementation shown in FIG. 18, the “up” signal of the phase comparator 4821 is never active and accordingly remains unconnected in the circuit; likewise, the “down” signal of the phase comparator 4822 is never active and accordingly remains unconnected in the circuit. FIG. 19 illustrates further details of the phase comparator 4821 of the phase detector 482 shown in FIG. 18 (the phase comparator 4822 is configured similarly to the comparator 4821). As shown in FIG. 19, the phase comparator 4821 includes two D-flip flops and a logic AND gate coupled between the respective Q outputs and reset inputs (R) of the flip-flops.

[0163] In one aspect of the embodiment of FIG. 18, the up signal from the comparator 4822 periodically activates transistor 4824, based on the amount of phase lead between $V_2(\omega)$ and $V(\omega)$, to allow the current I to be sourced by a current source 4823; in this manner, with reference again to FIG. 17, the capacitors of the low pass filter 484 are “pumped” with current based on the amount of phase lead between $V_2(\omega)$ and $V(\omega)$. Similarly, the down signal from the comparator 4821 periodically activates transistor 4825, based on the amount of phase lag between $V_1(\omega)$ and $V(\omega)$, to draw current from the capacitors of the low pass filter (to ground) based on the amount of phase lag between $V_1(\omega)$ and $V(\omega)$. At steady state, the combined activity of the pumping and drawing of current results in a net current I equal to zero, corresponding to the condition $\theta_2=\theta_1$.

[0164] FIG. 20 illustrates an alternative arrangement of RF/detection components 480A for facilitating sample detection according to another embodiment of the present disclosure. The arrangement of FIG. 20 represents a homodyne detection system in which two voltage controlled oscillators VCO (I) and VCO(Q) of a frequency synthesizer 4802 generate $\sin \omega t$ (in-phase, or I) and $\cos \omega t$ (quadrature-phase, or Q) signals, respectively. The in-phase (sin) RF signal excites the microcoil 212, which then modifies the excitation signal’s phase and amplitude. The response of the microcoil (output of the low-noise amplifier, or LNA) is then multiplied by the original in-phase signal in Mixer 1, and multiplied by the quadrature-phase signal in Mixer 2. The DC output of Mixer 1 (OUT 1) is proportional to the parasitic resistance R_L of the microcoil, while the DC output of Mixer 2 (OUT 2) is proportional to the inductance L of the