

[0173] In various implementations, the accuracy and long-term stability of the temperature regulator may be affected by mismatching of integrated components, drift of component parameters, 1/f (flicker) noise, and mechanical stress. To improve the accuracy of the temperature regulator loop, in some embodiments various conventional analog integrated circuit design techniques may be utilized, such as auto-zeroing, adaptive calibration and dynamics element matching, and signal-chopping and averaging.

#### [0174] V. Microfluidic System

[0175] With reference again to FIGS. 1 and 2, once an IC chip 102 including one or more of field generating components 200, field control components 400 and temperature regulation components 500 is fabricated, a microfluidic system 300 may be coupled to the IC chip 102 to form the hybrid system 100. As discussed above in Section I, according to one embodiment the microfluidic system 300 may be configured as a relatively simple chamber or reservoir for holding liquids containing samples of interest. For example, as illustrated generically in FIGS. 1 and 2, a microfluidic reservoir having an essentially rectangular volume may include access conduits 302 and 304 to facilitate fluid flow into and out of the reservoir. Alternatively, the microfluidic system may have a more complex arrangement including multiple conduits or channels in which liquids containing samples may flow, as well as various components (e.g., valves, mixers) for directing flow. In various embodiments, the microfluidic system 300 may be fabricated on top of an IC chip 102 containing other system components, once the semiconductor fabrication processes are completed, to form the hybrid system 100; alternatively, the microfluidic system 300 may be fabricated separately (e.g., using soft lithography techniques) and subsequently attached to one or more IC chips containing other system components to form the hybrid system 100.

[0176] In other aspects of the embodiment shown in FIG. 1, the electric and/or magnetic field-generating components 200 of the hybrid system 100 may be disposed with respect to the microfluidic system 300 in a variety of arrangements so as to facilitate interactions between generated fields and samples contained in (or flowing through) the microfluidic system. In various implementations, the field-generating components 200 may be disposed proximate to the microfluidic system along one or more physical boundaries of the microfluidic system and arranged so as to permit field-sample interactions along one or more spatial dimensions relative to the microfluidic system. In general, according to the various concepts discussed herein, samples of interest may be moved through the microfluidic system along virtually any path, trapped or held at a particular location, and in some cases rotated, under computer control of the electric and/or magnetic fields generated by the field-generating components 200. In this manner, the topology of a “virtual micro-scale plumbing system” for samples of interest may be flexibly changed for a wide variety of operations based on the programmability and computer control afforded, for example, by the processor(s) 600. This provides an extremely powerful tool for precision cell/object manipulation in both relatively simple and more sophisticated operations.

[0177] Generally, the top layer of an CMOS chip includes a silicon nitride or polyimide passivation layer, whose

purpose is to prevent chemical elements such as sodium from penetrating into the chip. According to one embodiment, a microfluidic system 300 may be further fabricated on the top of the CMOS chip passivation layer, wherein the microfluidic system includes micropatterned polyimide sidewalls in desired shapes so as to form channels, or “mini canals,” to guide samples. FIGS. 22-26 illustrate various process steps involved in fabricating a polyimide-based microfluidic system as part of a hybrid system according to one embodiment of the present disclosure.

[0178] In particular, FIG. 22 shows a portion of a semiconductor substrate 104 including a single chip 102. In one aspect, the portion of the substrate 104 illustrated in FIG. 22 has been diced from a larger semiconductor wafer in which have been fabricated multiple chips 102; in one exemplary implementation, each chip 102 has dimensions on the order of 2 millimeters by 5 millimeters, and the wafer substrate may be diced into portions having dimensions on the order of 15 millimeters by 25 millimeters.

[0179] Once diced, the respective substrate portions 104 each including a single chip 102 may be spin-coated with polyimide and then patterned using conventional lithography techniques. Since the CMOS chip surface layer generally includes a polyimide passivation layer, micropatterned polyimide sidewalls can be fabricated with good adhesion to the similar-material passivation layer. FIG. 23 illustrates an example of a polyimide layer 310 on top of the substrate 104, wherein the polyimide layer includes a fluidic channel 316 and two portholes 320 patterned using conventional lithography techniques. In various exemplary implementations, the coating and patterning process for the polyimide layer may be configured to form a height and width for the fluidic channel 316 in a range from a few microns to a few thousands of microns depending on the requirements of a given application.

[0180] After the fabrication of the fluidic channel 316 in the polyimide layer 310, according to one embodiment the surface of the fluidic channel may be optionally coated (e.g., spin-coated) with a thin layer of polydimethylsiloxane, or PDMS. PDMS is a biocompatible material whose surface can be functionalized to either encourage or prevent cell adhesion. For example, in one aspect of this embodiment, treating the oxidized surface of polymerized PDMS with Fibronectin (FN) makes it amenable to micro-patterning of extracellular matrix proteins to facilitate cell adhesion and spreading. In another aspect, treating the surface of PDMS with Pluronic F127 can block protein absorption, thus preventing the adhesion of cells. These respective characteristics may facilitate different aspects of guiding biological samples down the microfluidic channels of a cell sorter according to one embodiment of the present disclosure (discussed further below in Section VI), and for directing the cells to specific locations during two-dimensional micro-scale tissue assembly according to another embodiment of the present disclosure (also discussed further below in Section VII). In various implementations, PDMS may be spin-coated to micron-thickness layers onto the surface of the fluidic channel, without compromising sample manipulation or imaging.

[0181] As illustrated in FIG. 24, an appropriately shaped cover slip 312 (e.g., a glass cover slip) may be coupled to the polyimide layer 310 to form a microfluidic chamber or