

channel. In one aspect, the surface of the cover slip to be joined to the polyimide layer may be coated with a negative photoresist or ultraviolet curable epoxy **314** (e.g., SU-8, available from Microchem, Inc. of Newton, Mass.) to facilitate a seal between the cover slip and the polyimide layer (e.g., via curing of the assembly with ultraviolet light). **FIG. 25** illustrates the completed assembly of the cover slip **312** attached to the polyimide layer **312** so as to enclose the fluidic channel **316** and hence form the microfluidic system **300**.

[**0182**] Finally, as illustrated in **FIG. 26**, access conduits **302** and **304** are coupled to the portholes **320** of the assembly via tube fittings **305** to complete the microfluidic system **300**. In one implementation, a UV curable photoresist or epoxy again may be used to bond the tube fittings and conduits to the assembly. In **FIG. 26**, a portion of the conduit **304** is cut away in cross-section to illustrate the flow of fluid through the microfluidic system of the hybrid system **100**.

[**0183**] **FIGS. 27-32** illustrate various process steps involved in fabricating the microfluidic system **300** based on patterning of ultraviolet curable epoxy, according to another embodiment of the present disclosure. In this embodiment, with reference first to **FIG. 27**, an individual IC chip **102** (e.g., having a dimension on the order of approximately 2 millimeters by 5 millimeters, with a thickness of approximately 270 micrometers) is glued to a silicon substrate **1040** that is different from the substrate from which the IC chip was fabricated. Stated differently, in this embodiment, IC chips are diced from a larger wafer in which they were fabricated to a size that is essentially equal to their fabrication footprint in the wafer (i.e., no extra substrate surrounding the area of the chip). Chips diced in this manner are then adhered to another larger silicon substrate **1040** (e.g., having a dimension on the order of 25 millimeters by 25 millimeters), wherein the larger substrate may include electrodes fabricated thereon to facilitate electrical connections to the IC chip. In one aspect, the substrate **1040** may serve as the hybrid system's package substrate **110** (see **FIG. 2**).

[**0184**] As illustrated in **FIG. 28**, in this embodiment the assembly of the IC chip **102** and substrate **1040** then are spin-coated with a first layer **318** of ultraviolet curable epoxy (e.g., SU-8) to a thickness that is slightly thicker than the thickness of the IC chip **102** (e.g., approximately 300 micrometers). Via conventional optical lithography techniques, a number of portholes **320** are patterned in the first layer, and the patterned layer is baked (e.g., a post-exposure bake at 95 Celsius for 30 minutes) but not developed. Subsequently, as shown in **FIG. 29**, a second layer **322** of ultraviolet curable epoxy is spin-coated (e.g., to a thickness of approximately 100 micrometers) and patterned by optical lithography to form the sidewalls of the fluidic channel **316** and the portholes **320**. As with the first layer **318**, the second layer **322** is post-exposure baked, and then the second layer is developed to form the fluidic channel **316**. The development of the second layer exposes the porthole patterns of the first layer **318**, which is then also developed to complete the formation of the portholes **320**, as shown in **FIG. 30**.

[**0185**] Next, as illustrated in **FIG. 31**, a glass or plastic cover slip **312** is coated with a thin (e.g., 50 micrometer) layer of ultraviolet curable epoxy, cut into an appropriate shape, and placed on top of the patterned assemble. The assembled hybrid system **100** (minus the access conduits),

as shown in **FIG. 32**, is heated at 75 Celsius for approximately 10 minutes to soften the epoxy coated on the cover slip **312** and seal gaps at the junction of the cover slip and the second epoxy layer. Subsequently, the assembled device is blank-exposed with ultraviolet light and post-exposure baked to cure the bonding between the cover slip and the fluidic channel sidewalls. Access conduits then are connected to the assembly in a manner similar to that discussed above in connection with **FIG. 26**.

[**0186**] According to another embodiment, the hybrid system **100** shown in **FIGS. 1 and 2** may be implemented by fabricating the microfluidic system **300** separately using PDMS and soft lithography techniques, and subsequently attaching the microfluidic system to the IC chip **102** (details of soft lithography techniques suitable for this embodiment are discussed in the references entitled "Soft Lithography," by Younan xia and George M. Whitesides, published in the Annual Review of Material Science, 1998, Vol. 28, pages 153-184, and "Soft Lithography in Biology and Biochemistry," by George M. Whitesides, Emanuele Ostuni, Shuichi Takayama, Xingyu Jiang and Donald E. Ingber, published in the Annual Review of Biomedical Engineering, 2001, Vol. 3, pages 335-373; each of these references is incorporated herein by reference). **FIGS. 33-38** illustrate various process steps involved in fabricating the microfluidic system **300** based on such soft lithography techniques.

[**0187**] As shown in **FIGS. 33 and 34**, a silicon substrate is spin-coated with an ultraviolet curable epoxy **332** and patterned using a photomask **330** via conventional optical lithography techniques to produce a fluidic channel mold **334**. In **FIG. 35**, a PDMS layer **336** is cast-coated on the mold and heat-cured. As shown in **FIG. 36**, the cured PDMS layer is then peeled off the mold, with the impression of a fluidic channel **316** formed therein. The PDMS layer is cut into a desired shape, and bored with portholes **320** to form the microfluidic system **300**. In **FIG. 37**, a substrate **1040** to which an IC chip **102** has been attached is coated with a thin (e.g., 50 to 100 nanometers) layer **338** of Silicon Dioxide to promote bonding between the chip/substrate assembly and the PDMS microfluidic system **300**. The surfaces to be bonded of the PDMS microfluidic system **300** and the chip/substrate assembly are treated with an oxygen plasma to "activate" the surfaces for bonding upon the application of pressure, and in **FIG. 38** the activated surfaces are bonded together to form the hybrid system **100** (minus the access conduits).

[**0188**] In sum, according to various embodiments discussed above, an overall fabrication process for a CMOS/microfluidic hybrid system may include the following steps, in an appropriate order depending on the particular technique used: 1) silicon foundry fabrication of CMOS chip including microcoil array, digital switching network, imaging (e.g. RF) electronics and related circuitry, and temperature regulation electronics; 2) optional Permalloy deposition in appropriate microcoils to increase magnetic field strength; 3) fabrication of the microfluidic system (e.g., either on the chip directly via polyimide-based or ultraviolet epoxy-based techniques or separately with soft lithography PDMS mold); 4) PDMS coating of the CMOS chip surface with various agents for biocompatibility; 5) application of cover slip to form fluidic channel(s)/chamber; and 6) assembly of the