

the optical signal emitter is fanned-out by the at least one optical distributing element of one of the optics and broadcast to one of the plurality of receivers of all of the plurality of nodes by the optical collecting element of all of the plurality of optics. According to another aspect of the invention, a method comprises operating a broadcast optical interconnect including: fanning-out an optical signal from an optical signal emitter, of one of a plurality of nodes, with an optical distributing element of one of a plurality of optics; and substantially simultaneously broadcasting the optical signal to one of a plurality of receivers of all of the plurality of nodes with an optical collecting element of all of the plurality of optics, wherein the plurality of optics are positioned to define an optics array, the plurality of receivers are positioned to define a receiver array that corresponds to the optics array and the plurality of nodes are positioned to define a node array that substantially corresponds to the receiver array and the optics array.

[0025] These, and other, aspects of the invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating various embodiments of the invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many substitutions, modifications, additions and/or rearrangements may be made within the scope of the invention without departing from the spirit thereof, and the invention includes all such substitutions, modifications, additions and/or rearrangements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The drawings accompanying and forming part of this specification are included to depict certain aspects of the invention. A clearer conception of the invention, and of the components and operation of systems provided with the invention, will become more readily apparent by referring to the exemplary, and therefore nonlimiting, embodiments illustrated in the drawings, wherein identical reference numerals designate the same elements. The invention may be better understood by reference to one or more of these drawings in combination with the description presented herein. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale.

[0027] FIG. 1 illustrates a schematic perspective view of a subassembly including a mirror and lens array, representing an embodiment of the invention.

[0028] FIGS. 2A and 2B illustrate schematic perspective views of light rays from an emitter on a wafer opposite a mirror without (FIG. 2A) and with (FIG. 2B) a diverging lens, representing an embodiment of the invention.

[0029] FIG. 3 illustrates a schematic cross sectional view of light rays from an emitter through an unfolded wafer-mirror-lens array assembly, representing an embodiment of the invention.

[0030] FIG. 4 illustrates a schematic normal view of a composite lens assembly including a converging lens array and a diverging lens array, representing an embodiment of the invention.

[0031] FIG. 5 illustrates a schematic perspective view of the composite lens assembly shown in FIG. 4, representing an embodiment of the invention.

[0032] FIG. 6 illustrates a schematic normal view of an alternative composite optic including a converging lens and a diverging element in coaxial alignment with the converging lens, representing an embodiment of the invention.

[0033] FIG. 7A illustrates a schematic perspective views of an enclosed optical interconnect assembly including a heat exchanger, a power grid, a circuit wafer, a lens array and a mirror, representing an embodiment of the invention.

[0034] FIGS. 7B-7C illustrate schematic side (FIG. 7B) and normal (FIG. 7C) views of the enclosed optical interconnect assembly shown in FIG. 7A, representing an embodiment of the invention.

[0035] FIG. 8 illustrate a schematic normal view of a circuit wafer including a plurality of computer nodes each of which includes four optical signal sources (emitters), representing an embodiment of the invention.

[0036] FIGS. 9A and 9B illustrate schematic normal (FIG. 9A) and side (FIG. 9B) views of an individual computer node including four optical signal sources, representing an embodiment of the invention.

[0037] FIG. 10 illustrates a schematic perspective view of a power supply bus bar assembly, representing an embodiment of the invention.

[0038] FIG. 11 illustrates a schematic perspective view of two substantially orthogonal components of a light baffle assembly, representing an embodiment of the invention.

[0039] FIG. 12 illustrates a schematic perspective view of a light baffle assembly coupled to a plurality of individual computer nodes arranged in a wafer configuration, representing an embodiment of the invention.

[0040] FIG. 13 illustrates a schematic side view of a system including an optical computer assembly with a partially transmissive mirror coupled to an interface array via an optical link, representing an embodiment of the invention.

[0041] FIG. 14 illustrates a schematic side view of an interface array subassembly, representing an embodiment of the invention.

[0042] FIGS. 15A-15C illustrate schematic side views of three optical computer meta-assemblies, representing embodiments of the invention.

[0043] FIG. 16 illustrates a schematic side view of a systolic optical computer meta-assembly including four optical computers, representing an embodiment of the invention.

[0044] FIG. 17 illustrates a schematic side view of fan-out (broadcast) from an optical signal emitter via a diverging lens, representing an embodiment of the invention.

[0045] FIG. 18 illustrates a schematic side view of convergence from fan-out via a plurality of converging lenses, representing an embodiment of the invention.

[0046] FIG. 19 illustrates a schematic side view of convergence from a multiplicity of fan-outs via a plurality of converging lenses, representing an embodiment of the invention.

[0047] FIGS. 20A and 20B illustrate schematic normal views of single emitter modules having detector arrays