

deposited on top of M1. Poly-Si portion **1203** and an additional poly-Si portion are also shown in FIG. **20C**.

[0130] FIG. **20D** shows a side view of pixel **1101** along the line shown in FIG. **19**. The M1 layer shown in FIG. **20D** includes gate line portion **1113a**, gate **1105a**, and yVcom portion **1123a**, which includes an intersection with xVcom portion **1121a**. Connections **1301** and **1302** contact connection points **1141** and **1143**, respectively, of yVcom portion **1123a**. FIG. **20D** also shows a gate insulator layer **2005** and poly-Si portion **1209**. The M2 layer shown in FIG. **20D** includes yVcom portion **1423a**, which connects with connection **1301** at connection point **1441**, and yVcom portion **1423b**, which connects with connection **1302** at connection point **1443**. The vertical common line, yVcom **1123** (shown in FIG. **20D** as dashed lines) runs through pixel **1181** as yVcom portion **1423a**, connection **1301**, yVcom portion **1123a**, connection **1302**, and yVcom portion **1423b**. FIG. **20D** also shows a portion of an adjacent pixel that includes structure identical to pixel **1101**. In particular, the adjacent pixel includes a yVcom portion that is connected, via a connection, to an xVcom portion. Thus, FIG. **20D** illustrates that a xVcom portion **1121a** can be connected to an adjacent pixels xVcom portion with a yVcom line.

[0131] FIGS. **21** and **22** show a comparative analysis of the storage capacitance of pixels **1101** and **1102**. The total storage capacitance (C_{store}) of pixel **1102** is:

$$C_{store}=C_{M1/M2}+C_{M1/ITO} \quad (1)$$

[0132] where: $C_{M1/M2}$ is the capacitance of the overlapping M1 and M2 layers, such as upper electrode **1457a** and lower electrode **1157b** of pixel **1102**, and

[0133] $C_{M1/ITO}$ is the capacitance between overlapping areas of the first metal layer and the transparent conductor layer.

[0134] For example, FIG. **21** shows the overlapping areas of the first and second metal layers that result in the capacitance $C_{M1/M2}$. As shown in FIG. **21**, $C_{M1/M2}$ of pixel **1102** results from an overlap of approximately 360 square micrometers of the first and second metallic layers. Referring now to FIG. **22**, the highlighted portions of pixel **1102** show the overlapping regions of the first metallic layer and the transparent conductor layer that result in $C_{M1/ITO}$. As shown in FIG. **22**, the total overlap is approximately 360 square micrometers.

[0135] In contrast, the total capacitance of pixel **1101** is:

$$C_{store}=C_{M1/M2}+C_{M1/ITO}+C_{M2/ITO} \quad (2)$$

[0136] where: $C_{M1/M2}$ and $C_{M1/ITO}$ are defined as above, and

[0137] $C_{M2/ITO}$ is the capacitance resulting from the overlap of the second metallic layer and the transparent conductor layer.

[0138] The additional term in the storage capacitance equation for pixel **1101**, $C_{M2/ITO}$, results from the additional areas of the second metallic layer in pixel **1101** that overlap with the transparent conductor layer. FIGS. **21** and **22** show the areas of overlapping metal in pixel **1101** that result in the terms of equation **2**. FIG. **21** shows an overlapping region of the first and second metallic layers in pixel **1101** that equals approximately 503 square micrometers. FIG. **22** shows overlapping regions of the first metallic layer and the transparent conductor layer in pixel **1101** that equals approximately 360 square micrometers. FIG. **22** also shows an overlapping region of the second metallic layer and the transparent conductor layer that equals approximately 81 square micrometers. Thus, it is

apparent from FIGS. **21** and **22** that, while the area of overlap of the first and second metallic layers of pixel **1101** is less than the corresponding area of pixel **1102**, pixel **1101** has an extra area overlap that pixel **1102** does not. In particular, the overlap of the second metallic layer and the transparent conductor layer in pixel **1101** contributes an additional 81 square micrometers, which in turn contributes an additional amount of capacitance to the storage capacitance of pixel **1101**.

[0139] FIG. **23** illustrates aperture ratio estimations for pixels **1101** and **1102**. Pixel **1101** has an aperture ratio of 41.4%. Pixel **1102** has an aperture ratio of 44.4%.

[0140] FIG. **24** illustrates an example modification according to embodiments of the invention. As a result of the modification, the aperture ratios of the different pixels in a system may be made more similar, which may improve the appearance of the display. Similar to pixel **1102**, pixels **2401** and **2405** do not include connection portions in the y-direction. Pixel **2403**, on the other hand, does include a connection portion in the y-direction, similar to pixel **1101**.

[0141] FIGS. **25-34** are directed to an example IPS LCD display using low temperature polycrystalline silicon (LTPS). An example process of manufacturing an IPS LCD display using LTPS according to embodiments of the invention will now be described with reference to FIGS. **25-31**. The figures show various stages of processing of two pixels, a pixel **2501** and a pixel **2502**, during the manufacture of the IPS LCD display using LTPS. The resulting pixels **2501** and **2502** form electrical circuits equivalent to pixels **101** and **102**, respectively, of FIG. **1**. Because the stages of processing shown in FIGS. **25-30** are the same for pixel **2501** and pixel **2502**, only one pixel is shown in each of these figures. However, it is understood that the stages of processing show in FIGS. **25-30** apply to both pixel **2501** and pixel **2502**.

[0142] FIG. **25** shows the patterning of a layer of poly-Si of pixels **2501** and **2502**. Semiconductor portions **2505**, **2507**, and **2509** form the active region of a TFT, and serve as source, gate, and drain, respectively.

[0143] FIG. **26** shows a subsequent patterning step in the process of manufacturing pixels **2501** and **2502**, in which a first metal layer (M1) of pixels **2501** and **2502** is formed. As shown in FIG. **26**, the M1 layer for the pixels **2501/2502** includes a gate **2605a**, a portion **2613a** of a gate line **2613** (shown as dotted lines), and a portion **2621a** of xVcom **2621**. Portion **2621a** includes a connection point **2623**. Gate line **2613** and xVcom **2621** run through pixels that are adjacent in the x-direction.

[0144] FIG. **27** shows vias **2701**, **2703**, and **2705** formed in pixels **2501/2502** for connections to portion **2505**, portion **2509**, and connection point **2623**, respectively.

[0145] FIG. **28** shows patterning of a second metal layer (M2) of pixels **2501/2502**. As shown in FIG. **28**, the M2 layer of the pixels forms a portion **2817a** of a color data line **2817** (shown as a dotted line in FIG. **28**), which could carry red, green, or blue color data, for example. Portion **2817a** includes a connection **2819** that connects to portion **2505** through via **2701**. The M2 layer also forms a connection **2821** with portion **2509** through via **2703**, and forms a connection **2823** to connection point **2623** through via **2705**.

[0146] FIG. **29** shows a first layer of transparent conductive material, such as ITO, formed on pixels **2501/2502**. The first transparent conductor layer includes a pixel electrode **2901**. FIG. **29** also shows a portion **2905** of a pixel electrode of a pixel adjacent in the x-direction, and a portion **2907** of a pixel electrode of a pixel adjacent in the y-direction. FIG. **29** also