an emitter region spaced apart from the second body region, the emitter region having the first conductivity type,

a base region under the emitter region and surrounding the emitter region, the base region having the second conductivity type, and

the second drain region.

6. The semiconductor device as claimed in claim **5**, wherein the bipolar transistor includes an epitaxial layer under the base region.

7. The semiconductor device as claimed in claim **5**, wherein the base region is in a non-overlapping relationship with the second deep well.

8. The semiconductor device as claimed in claim **5**, wherein a doping concentration of the base region is higher than a doping concentration of the second deep well and lower than a doping concentration of the second body region.

9. The semiconductor device as claimed in claim **5**, wherein a first distance from a bottom surface of the substrate to a bottom surface of the base region is greater than a second distance from the bottom surface of the substrate to a bottom surface of the second body region.

10. The semiconductor device as claimed in claim **5**, wherein:

the first LDMOS device includes a first drift region that is under the first isolation region and the first drain region and that surrounds the first isolation region and the first drain region, the first drift region having the first conductivity type, and

the second LDMOS device includes a second drift region that is under the second isolation region and the second drain region and that surrounds the second isolation region and the second drain region, the second drift region having the first conductivity type.

11. The semiconductor device as claimed in claim **5**, wherein a length of the second isolation region is equal to or smaller than a length of the first isolation region.

12. The semiconductor device as claimed in claim **5**, wherein a second overlapping length between the second isolation region and the second deep well is equal to or greater than a first overlapping length between the first isolation region and the first deep well.

13. The semiconductor device as claimed in claim **5**, wherein a portion of the base region and a portion of the second deep well overlap each other.

14. The semiconductor device as claimed in claim **13**, wherein substantially an entire area of the base region is in a non-overlapping relationship with the second deep well.

15. The semiconductor device as claimed in claim **3**, wherein the bipolar transistor includes:

an emitter region in the second body region, the emitter region having the first conductivity type,

the second body region surrounding the emitter region, and

the second drain region.

16. A semiconductor device, comprising:

an output port including a first lateral double diffused metal oxide semiconductor (LDMOS) device; and

an electrostatic discharge protection device that includes a second LDMOS device and a silicon controlled rectifier and that protects the output port from electrostatic discharge,

a breakdown voltage of the second LDMOS device being equal to or lower than a breakdown voltage of the first LDMOS device.

17. The semiconductor device as claimed in claim **16**, wherein the silicon controlled rectifier includes a NPN bipolar transistor and a PNP bipolar transistor.

18. The semiconductor device as claimed in claim **17**, wherein the first LDMOS device includes:

a first gate on a substrate,

a first source region at one side of the first gate, the first source region having a first conductivity type,

a first body region under the first source region and surrounding the first source region, the first body region having a second conductivity type, the second conductivity type being different from the first conductivity type,

a first body contact region in the first body region, the first body contact region having the second conductivity type,

a first drain region at another side of the first gate, the first drain region having the first conductivity type,

a first isolation region in the substrate between the first source region and the first drain region, the first isolation region overlapping a portion of the first gate,

a first deep well under the first body region, the first deep well having the second conductivity type, and

a first buried layer under the first deep well, the first buried layer having the first conductivity type.

19. The semiconductor device as claimed in claim **18**, wherein the second LDMOS device includes:

a second gate on the substrate,

a second body region at one side of the second gate, the second body region having the second conductivity type,

a second body contact region in the second body region, the second body contact region having the second conductivity type,

a second drain region at another side of the second gate, the second drain region having the first conductivity type,

a second isolation region in the substrate between the second body region and the second drain region, the second isolation region overlapping a portion of the second gate,

a second deep well under the second body region, the second deep well having the second conductivity type, and

a second buried layer under the second deep well, the second buried layer having the first conductivity type.

20. The semiconductor device as claimed in claim **19**, wherein a length of the second isolation region is equal to or smaller than a length of the first isolation region.

21. The semiconductor device as claimed in claim **19**, wherein a second overlapping length between the second isolation region and the second deep well is equal to or greater than a first overlapping length between the first isolation region and the first deep well.

22. The semiconductor device as claimed in claim **19**, wherein:

the NPN bipolar transistor includes an emitter region having the first conductivity type and a base region having the second conductivity type, the emitter region having the first conductivity type being spaced apart from the second body region, and the base region being under the emitter region of the first conductivity type and surrounding the emitter region of the first conductivity type and the second drain region, and