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(54) **METHODS OF DESIGNING A LAYOUT OF A SEMICONDUCTOR DEVICE INCLUDING FIELD EFFECT TRANSISTOR AND METHODS OF MANUFACTURING A SEMICONDUTOR DEVICE USING THE SAME**

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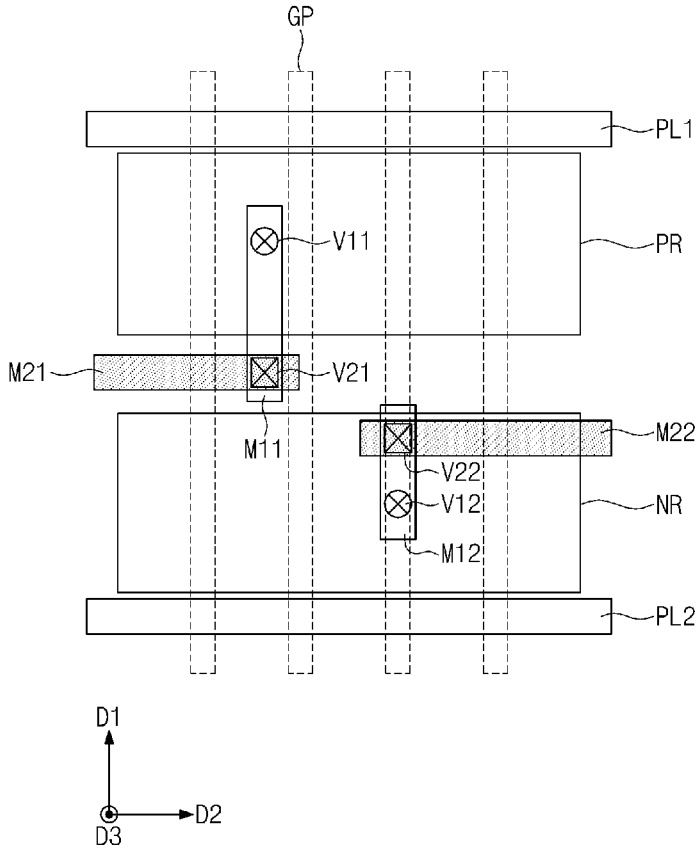
(57) **ABSTRACT**

A method of designing a semiconductor device includes preparing a standard cell layout including a layout out a preliminary pin pattern in at least one interconnection layout, performing a routing step to connect the preliminary pin pattern to a high-level interconnection layout, and generating a pin pattern in the interconnection layout, based on hitting information obtained at the completion of the routing step. The pin pattern is smaller than the preliminary pin pattern.