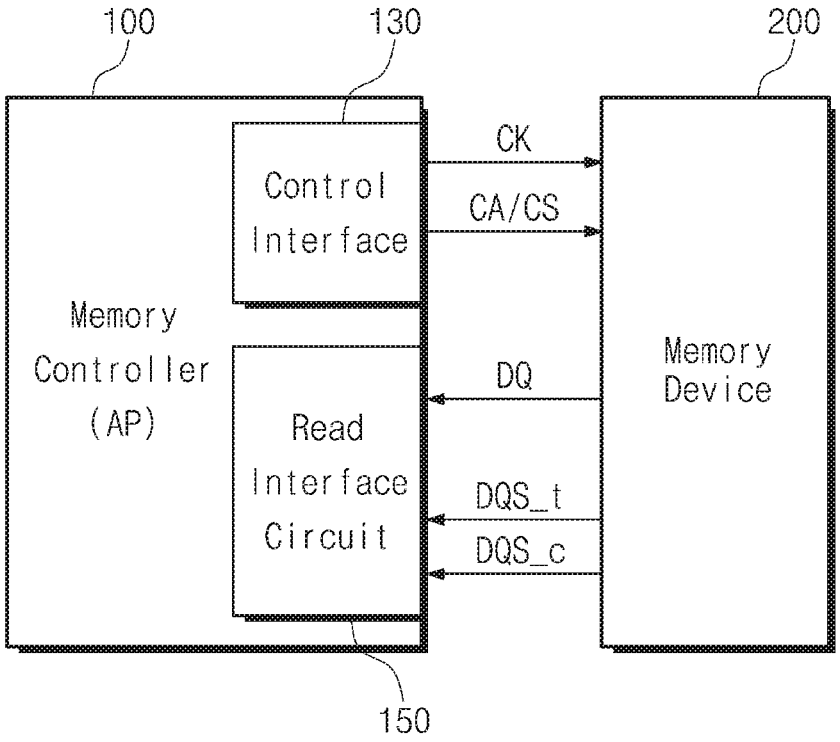
FIG. 1


100
130
200
Control Interface
CK
CA/CS
Memory Controller (AP)
Memory Device
DQ
Read Interface Circuit
DQS_t
DQS_c
150