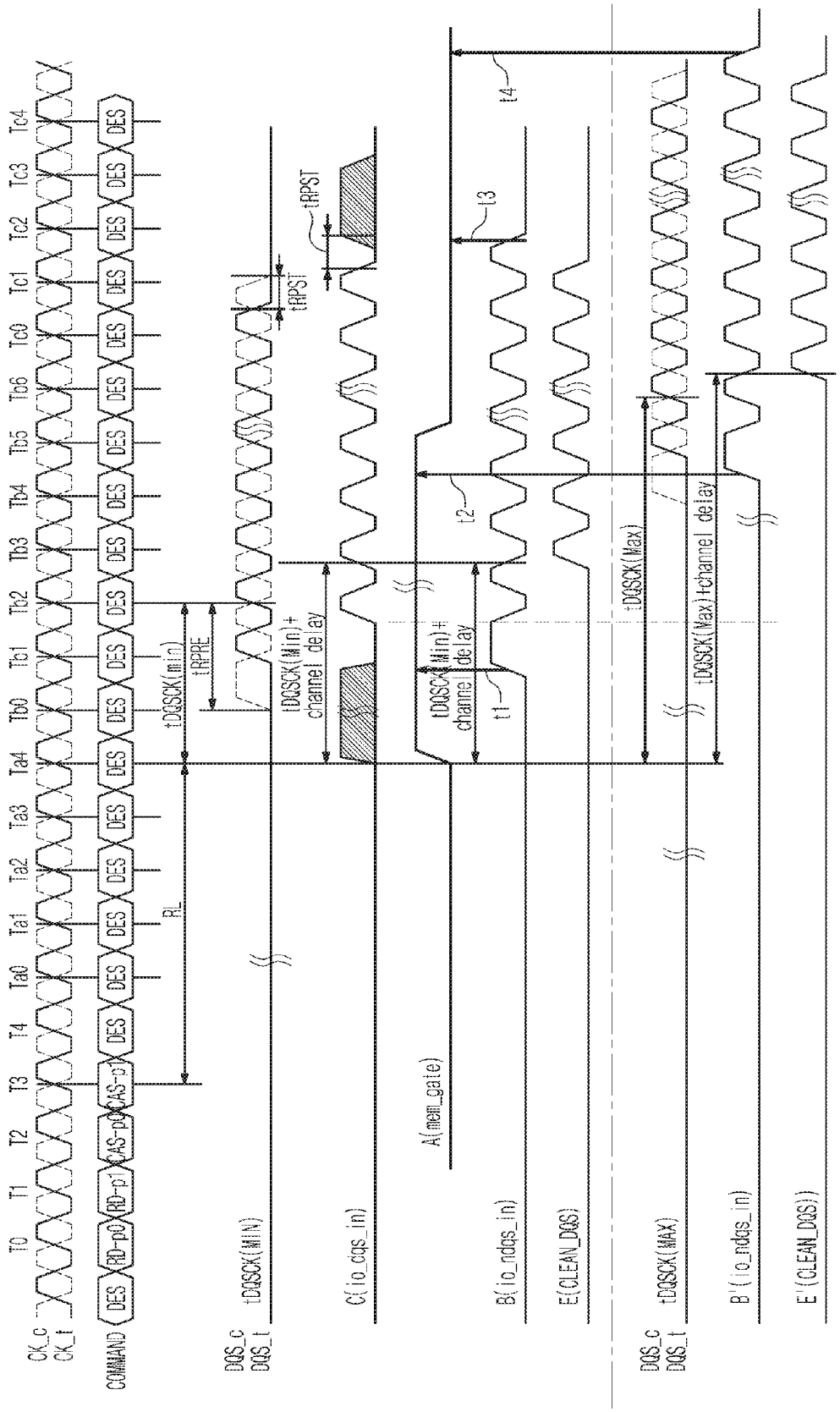
FIG. 3


CK_c
CK_t
COMMAND
DQS_c
DQS_t
T0
T1
T2
T3
T4
Ta0
Ta1
Ta2
Ta3
Ta4
Tb0
Tb1
Tb2
Tb3
Tb4
Tb5
Tb6
Tc0
Tc1
Tc2
Tc3
Tc4
DES
RD-p0
RD-p1
CAS-p0
CAS-p1
RL
tDQSCK(MIN)
tRPRE
tDQSCK(Min)+ channel delay
tRPST
C(io_dqs_in)
A(mem_gate)
B(io_ndqs_in)
E(CLEAN_DQS)
t1
t2
t3
t4
tDQSCK(Max)
tDQSCK(Max)+channel delay
tDQSCK(MAX)
B'(io_ndqs_in)
E'(CLEAN_DQS)