

screen **100**, by a signal denoted COL\_EN\_N. When ROW\_EN\_N is low, any of the row LEDs whose corresponding bit in shift register **110** is set, issue a light pulse. Similarly, when COL\_EN\_N is low, any of the column LEDs whose corresponding bit in shift register **110** is set, issue a light pulse. Transistor **300** may be a low saturation voltage type transistor, such as the transistors manufactured by NXP Semiconductors of The Netherlands.

**[0098]** The magnitude of the current gated by transistor **300**, and issued by VROW, is determined by resistors R1, R2 and R3. Specifically, the current limit VROW, ignoring the base current, are given by:

$$I_{row} = \frac{+3V \frac{R2}{R2-R3} - U_{be}}{R1}$$

Where +3V is the input voltage to controller **150** (FIG. 6), and U<sub>be</sub> is the base-to-emitter voltage on transistor **300**.

**[0099]** Reference is now made to FIG. 13B, which is a diagram of alternative current limiters B, used for limiting and directing current to LEDs through VROW and VCOL, in accordance with an embodiment of the present invention. As in FIG. 13A, only one current limiter is shown in FIG. 13B, receiving input ROW\_EN and controlling current sent over VROW, and a similar current limiter (not shown) receives input COL\_EN and controls current sent of VCOL. The dotted portion of circuit **400** represents LED circuits, and the dotted line connected to the solid line corresponds to VROW.

**[0100]** Shown in FIG. 13B is a bandgap voltage stabilizer, D2, or such other voltage stabilizer, which has a contact voltage drop across it irrespective of the current flowing through it. As long as the current is above a holding current, the voltage across D2 is constant. Resistor R1 supplies a diode current and a base current of NPN transistor Q1. The constant diode voltage, denoted by VZ, applies across the base of Q1 and emitter resistor R2.

**[0101]** When circuit **400** is operational, the voltage across R2, denoted by VR2, is given by VR2=VZ-VBE, where VBE is the base-emitter drop of Q1. The emitter current of Q1, denoted by IE, which is also the current through R2, denoted by IR2, is given by

$$IR2 = \frac{VR2}{R2} = \frac{VZ - VBE}{R2}$$

Since VZ is constant, and VBE is approximately constant for a given temperature, it follows that VR2 is constant and IE is constant. Due to transistor action, current IE is approximately equal to the collector current of the transistor, denoted by IC, which is the current through the load. Thus, neglecting the output resistance of the transistor due to the Early effect, the load current is constant and the circuit operates as a constant current source.

**[0102]** Provided the temperature does not vary significantly, the load current is independent of the supply voltage, denoted by VR1, and the transistor's gain, R2, allows the load current to be set at any desired value. Specifically, R2 is given by

$$R2 = \frac{VZ - VBE}{IR2} \approx \frac{Vz - 0.65}{IR2}$$

Since VBE is generally 0.65V for silicon devices.

**[0103]** VBE is temperature dependent; namely, at higher temperatures, VBE decreases. VZ is also temperature dependent; namely, at higher temperatures, VZ also decreases. As such, circuit **400** is self regulating as both voltages grow or decline simultaneously, resulting in a substantially constant voltage VR2.

**[0104]** When issuing a light pulse, signal ROW\_EN is initially set to low. Capacitor C1 is also low, and begins to accumulate charge. Subsequently, ROW\_EN is briefly set to high, to activate the light pulse, and the charge on C1 rises accordingly. The presence of bandgap diode D1 ensures that the charge on C1 drops quickly when ROW\_EN is again set to low. As such, the presence of diode D1 protects circuit **400** from excessive charge that would otherwise result over the course of multiple pulses.

**[0105]** Resistance R1 is given by

$$R1 = \frac{VS - VZ}{IZ + K \cdot IB}$$

where IB is given by

$$IB = \frac{IC}{hFE(\min)} = \frac{IE}{hFE(\min)} = \frac{IR2}{hFE(\min)}$$

and hFE(min) is the lowest acceptable current gain for the specific transistor type being used. The parameter K ranges between 1.2 and 2.0, to ensure that R1 is sufficiently low and that IB is adequate.

**[0106]** v. PD Selector **170** and Shift Register **120**

**[0107]** Reference is now made to FIG. 14, which is a diagram of shift register **120** for an array of 16 PDs **140**, in accordance with an embodiment of the present invention. The PD shift register shown in FIG. 14 is similar to the LED shift register in FIG. 8. In contrast to LEDs **130**, PDs **140** are activated directly without intermediate switches such as switches A used with LEDs **130**. Shift register **120** is connected to controller **150** via the PD\_CTRL signal shown in FIG. 7. A description of the PD\_CTRL signal now follows.

**[0108]** Initially, the PD outputs are set to high. A value of 1 in at least one bit of shift register **120** (FIG. 5) activates at least one corresponding PD by setting its output low. The PD output signal is sent back to controller **150** via signal PDROW or PDCOL.

**[0109]** Reference is now made to FIG. 15, which illustrates a waveform for activating selected PDs, in accordance with an embodiment of the present invention. FIG. 15 illustrates the use of signals SI, SCK, RCK, SCLR\_N and OE\_N from FIG. 7.

**[0110]** At time t1, a low SCLR\_N signal sets all PD outputs low and clears shift register **120**. At time t2, a low SI signal enters an activation value of "1" into the beginning of shift register **120**. At each rising high edge of signal SCK, the data in shift register **120** is shifted further into the register, and a new bit value is entered in the beginning of the register. A