

the timing controller is configured to control timing so that the first output data group and the second output data group are simultaneously received by the output data buffer.

10. The display device of claim 7, wherein the timing controller comprises:

- a first port output terminal configured to transmit the first output data group at the first transmission speed; and
- a second port output terminal configured to transmit the second output data group at the second transmission speed.

11. The display device of claim 10, wherein the number of electrical interconnection lines through which the first port output terminal is connected to the first source driver circuit is less than the number of electrical interconnection lines through which the second port output terminal is connected to the second source driver circuit.

12. A display driving device comprising:

- a display panel comprising first and second pixel arrangement areas, each of the first and second pixel arrangement areas comprising a plurality of pixels arranged in areas in which a plurality of gate lines intersect a plurality of data lines;

- a data driving circuit comprising a first source driver circuit configured to output a first display data group to a data line of the first pixel arrangement area, and a second source driver circuit configured to output a second display data group to a data line of the second pixel arrangement area;

- a timing controller configured to array input data and configured to transmit output data to the data driving circuit at at least two transmission speeds, the timing controller being configured to generate timing control signals;

- a gate driving circuit configured to receive one of the timing control signals and configured to drive the plurality of gate lines of the display panel; and

- a voltage generating circuit configured to generate voltages for driving the display panel.

13. The display driving device of claim 12, wherein a printed circuit board (PCB) with the first source driver circuit formed thereon is connected to a PCB with the second source driver circuit formed thereon through a bridge cable.

14. The display driving device of claim 12, wherein a vertical or horizontal distance from the timing controller to the first source driver circuit is shorter than a vertical or horizontal distance from the timing controller to the second source driver circuit.

15. The display driving device of claim 14, wherein the amount of data of the first display data group is greater than the amount of data of the second display data group.

16. The display driving device of claim 14, wherein the first source driver circuit comprises at least one first source driver configured to support a first transmission speed,

the second source driver circuit comprises at least one second source driver configured to support a second transmission speed, and

the first transmission speed is higher than the second transmission speed.

17. The display driving device of claim 16, wherein each of the at least one first source driver and the at least one second source driver comprises data line driving circuits,

- each of the data line driving circuits is connected to a data line of one of the plurality of pixels of the display panel, and is configured to provide the output data, and

- the number of data line driving circuits of the first source driver is greater than the number of data line driving circuits of the second source driver.

18. The display driving device of claim 14, wherein the number of pixels of the first pixel arrangement area is greater than the number of pixels of the second pixel arrangement area.

19. A display driving device comprising:

- a display panel comprising first and second pixel arrangement areas, each of the first and second pixel arrangement areas comprising a plurality of pixels arranged in areas in which a plurality of gate lines intersect a plurality of data lines;

- a data driving circuit comprising a first source driver circuit configured to output a first display data group to data lines of the first pixel arrangement area, and a second source driver circuit configured to output a second display data group to data lines of the second pixel arrangement area; and

- a timing controller configured to array data that is input from an external device, to transmit a first output data group to the first source driver circuit at a first transmission speed, and to transmit a second output data group to the second source driver circuit at a second transmission speed,

- wherein the first transmission speed is higher than the second transmission speed.

20. The display driving device of claim 19, wherein the first source driver circuit comprises a first output data buffer circuit configured to receive the first output data group,

- the second source driver circuit comprises a second output data buffer circuit configured to receive the second output data group,

- the amount of data of the first output data group is greater than the amount of data of the second output data group, and

- the timing controller is configured to control reception timing so that a time period at which the first output data buffer circuit receives the first output data group is the same as a time period at which the second output data buffer circuit receives the second output data group.

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