

than the RF frequency (2.4 GHz in the case of Bluetooth) to avoid interference. Further, the controller **140** ensures that the edges of the clock do not generate harmonics that interfere with the 2.4 GHz frequency. In one implementation, the first harmonic of a 1.2 GHz signal is used as the 2.4 GHz carrier frequency.

[**0028**] When 2.4 GHz operation is desired, the clock is rapidly increased to 2.4 GHz with a suitable phase locked loop fed to both the processor core and the Bluetooth core. In one implementation, the edges of the clock signal generated by the PLL's voltage controlled oscillator are phase-modulated using a random-number sequencer in order to reduce the harmonic content of the resulting clock signal. The digital clock can be transformed into an analog carrier wave using a gaussian filter and a lowpass filter such as a high-order Chebyshev or Butterworth filter.

[**0029**] In one embodiment, the controller **140** varies the clock signal period to effectively spread the undesirable frequency harmonics spurs over the frequency band because the harmonic frequency created by the clock varies over time. The clock signal period can be varied using techniques such as those disclosed in U.S. Pat. No. 5,426,392 and U.S. Pat. No. 5,488,627, among others. The spurious signal energy at the nominal harmonic frequency is reduced and the energy is spread across the spectrum.

[**0030**] The clock trace can be used as an antenna, radiating the signal directly from its surface, removing the need for an external antenna. This system is adapted to work with transmitter with low output power levels, such as those specified by Bluetooth (0 dBm). The clock traces can also be used as a receive antenna to catch signals from a local radio source. The wiring traces act as an antenna, with the clock circuit spread out over the device. Since Bluetooth power output can be increased up to a watt, a Bluetooth™ transmitter can program devices even a few meters away using the clock trace antennas.

[**0031**] In addition to using clock traces and pads as an array of patch antennas, dedicated metal film lines on the device can be used. For instance, U.S. Pat. No. 5,381,157 to Shiga entitled "Monolithic microwave integrated circuit receiving device having a space between antenna element and substrate" uses a metal film constituting patch antennas about which are antenna elements of the planar antenna is also formed on the surface and is connected to circuit components by a first layer-metal line. The entire backside of the Shiga substrate is covered by a metal layer acting as a grounding conductor and connected to the first layer-metal line suitably by a via hole. The Shiga patch antennas have an air bridge structure as the metal film constituting the patch antennas is formed with a space above the surface of the substrate.

[**0032**] In one embodiment, the patch antenna can be used to get power off-chip, at least enough to power the processor clock and start the communication protocol for downloading data. For example, during wafer test, a high power 2.4 GHz signal can be beamed at the die, powering up the clock and carrying the data at the same time. The system can use Inductive Power Transfer with an AC-energized coil to create a magnetic field that couples with a receiving coil of an inductively powered device. The induced signal appearing at the output of the inductively powered device coil is then rectified and filtered to create a relatively constant DC

power source. Alternatively, as discussed in U.S. Pat. No. 6,047,214, Magnetic Vector Steering (MVS) and Half-Cycle Amplitude Modulation (HCAM) techniques can be used to enhance the powering and control of multiple arbitrarily oriented devices. Together, these techniques enable arbitrarily oriented devices to receive power and command, programming, and control information in an efficient manner. By steering the aggregate magnetic field from a near-orthogonal set of AC-energized coils, selected devices can be powered or communicated with at desired times.

[**0033**] Even though for most RF operations the 2.4 GHz carrier signal is frequency hopping within a range of 2.4-2.48 GHz, this variation is not a problem for a digital clock. The typical BPSK modulation used by the wireless transmission also varies the clock frequency, but the variation is slow as compared to the carrier (for example around 0.001 ratio), that the processor will not encounter glitches (other than within acceptable limits). Operating the radio and the micro-processor at the same frequency has the advantage of locking the high power RF signal in step with the digital clock, thus reducing commonly encountered problems such as VCO frequency pulling and ground bounce during the RF low-high transitions.

[**0034**] The high-density memory array core **170** can include various memory technologies such as flash memory and dynamic random access memory (DRAM), among others, on different portions of the memory array core. The reconfigurable processor core **150** can include one or more processors **151** such as MIPS processors and/or one or more digital signal processors (DSPs) **153**, among others. The reconfigurable processor core **150** has a bank of efficient processors **151** and a bank of DSPs **153** with embedded functions. These processors **151** and **153** can be configured to operate optimally on specific problems. For example, the bank of DSPs **153** can be optimized to handle discrete cosine transforms (DCTs) or Viterbi encodings, among others. Additionally, dedicated hardware **155** can be provided to handle specific algorithms in silicon more efficiently than the programmable processors **151** and **153**. The number of active processors is controlled depending on the application, so that power is not used when it is not needed. This embodiment does not rely on complex clock control methods to conserve power, since the individual clocks are not run at high speed, but rather the unused processor is simply turned off when not needed.

[**0035**] One exemplary processor embedded in the multi-processor core **150** includes a register bank, a multiplier, a barrel shifter, an arithmetic logic unit (ALU) and a write data register. The exemplary processor can handle DSP functions by having a multiply-accumulate (MAC) unit in parallel with the ALU. Embodiments of the processor can rapidly execute multiply-accumulate (MAC) and add-compare-subtract (ACS) instructions in either scalar or vector mode. Other parts of the exemplary processor include an instruction pipeline, a multiplexer, one or more instruction decoders, and a read data register. A program counter (PC) register addresses the memory system **170**. A program counter controller serves to increment the program counter value within the program counter register as each instruction is executed and a new instruction must be fetched for the instruction pipeline. Also, when a branch instruction is executed, the target address of the branch instruction is loaded into the program counter by the program counter