controller. The processor core **150** incorporates data pathways between the various functional units. The lines of the data pathways may be synchronously used for writing information into the core **150**, or for reading information from the core **150**. Strobe lines can be used for this purpose.

[**0036**] In operation, instructions within the instruction pipeline are decoded by one or more of the instruction decoders to produce various core control signals that are passed to the different functional elements of the processor core **150**. In response to these core control signals, the different portions of the processor core conduct processing operations, such as multiplication, addition, subtraction and logical operations. The register bank includes a current programming status register (CPSR) and a saved programming status register (SPSR). The current programming status register holds various condition and status flags for the processor core **150**. These flags may include processing mode flags (e.g. system mode, user mode, memory abort mode, etc.) as well as flags indicating the occurrence of zero results in arithmetic operations, carries and the like.

[**0037**] Through the router **190**, the multi-mode wireless communicator device **100** can detect and communicate with any wireless system it encounters at a given frequency. The router **190** performs the switch in real time through an engine that keeps track of the addresses of where the packets are going. The router **190** can send packets in parallel through two or more separate pathways. For example, if a Bluetooth™ connection is established, the router **190** knows which address it is looking at and will be able to immediately route packets using another connection standard. In doing this operation, the router **190** working with the RF sniffer **111** periodically scans its radio environment ('ping') to decide on optimal transmission medium. The router **190** can send some packets in parallel through both the primary and secondary communication channel to make sure some of the packets arrive at their destinations.

[**0038**] The reconfigurable processor core **150** controls the cellular radio core **110** and the short-range wireless transceiver core **130** to provide a seamless dual-mode network integrated circuit that operates with a plurality of distinct and unrelated communications standards and protocols such as Global System for Mobile Communications (GSM), General Packet Radio Service (GPRS), Enhance Data Rates for GSM Evolution (Edge) and Bluetooth™. The cell phone core **110** provides wide area network (WAN) access, while the short-range wireless transceiver core **130** supports local area network (LAN) access. The reconfigurable processor core **150** has embedded read-only-memory (ROM) containing software such as IEEE802.11, GSM, GPRS, Edge, and/or Bluetooth™ protocol software, among others.

[**0039**] In one embodiment, the cellular radio core **110** includes a transmitter/receiver section that is connected to an off-chip antenna (not shown). The transmitter/receiver section is a direct conversion radio that includes an I/Q demodulator, transmit/receive oscillator/clock generator, multi-band power amplifier (PA) and PA control circuit, and voltage-controlled oscillators and synthesizers. In another embodiment of transmitter/receiver section **112**, intermediate frequency (IF) stages are used. In this embodiment, during cellular reception, the transmitter/receiver section converts received signals into a first intermediate frequency (IF) by mixing the received signals with a synthesized local oscillator frequency and then translates the first IF signal to a second IF signal. The second IF signal is hard-limited and processed to extract an RSSI signal proportional to the logarithm of the amplitude of the second IF signal. The hard-limited IF signal is processed to extract numerical values related to the instantaneous signal phase, which are then combined with the RSSI signal.

[**0040**] For voice reception, the combined signals are processed by the processor core **150** to form PCM voice samples that are subsequently converted into an analog signal and provided to an external speaker or earphone. For data reception, the processor simply transfers the data over an input/output (I/O) port. During voice transmission, an off-chip microphone captures analog voice signals, digitizes the signal, and provides the digitized signal to the processor core **150**. The processor core **150** codes the signal and reduces the bit-rate for transmission. The processor core **150** converts the reduced bit-rate signals to modulated signals such as I,I,Q,Q modulating signals, for example. During data transmission, the data is modulated and the modulated signals are then fed to the cellular telephone transmitter of the transmitter/receiver section.

[**0041**] Turning now to the short-range wireless transceiver core **130**, the short-range wireless transceiver core **130** contains a radio frequency (RF) modem core **132** that communicates with a link controller core **134**. The processor core **150** controls the link controller core **134**. In one embodiment, the RF modem core **132** has a direct-conversion radio architecture with integrated VCO and frequency synthesizer. The RF-unit **132** includes an RF receiver connected to an analog-digital converter (ADC), which in turn is connected to a modem **116** performing digital modulation, channel filtering, AFC, symbol timing recovery, and bit slicing operations. For transmission, the modem is connected to a digital to analog converter (DAC) that in turn drives an RF transmitter.

[**0042**] The link controller core **134** provides link control function and can be implemented in hardware or in firmware. One embodiment of the core **134** is compliant with the Bluetooth™ specification and processes Bluetooth™ packet types. For header creation, the link controller core **134** performs a header error check, scrambles the header to randomize the data and to minimize DC bias, and performs forward error correction (FEC) encoding to reduce the chances of getting corrupted information. The payload is passed through a cyclic redundancy check (CRC), encrypted/scrambled and FEC-encoded. The FEC encoded data is then inserted into the header.

[**0043**] **FIG. 2** shows one implementation of a clock controller **140**. The clock controller **140** receives a reference clock signal **141**. The reference clock signal **141** can be generated off-chip, or alternatively, can be generated on-chip using an on-chip oscillator that can be crystal controlled, resistive-capacitive (RC) controlled, or can be a ring-oscillator. The reference signal **141** is provided to a frequency multiplier **142**. In one embodiment, the frequency multiplier **142** generates a clock signal at 2.4 GHz. The clock signal can be supplied to both the processor core and a local oscillator for the wireless core. Since current generation of microprocessors uses frequencies in excess of 1 GHz, easily reaching the 2.4 GHz required for Bluetooth and 802.11 operation, the master clock can then be used to power the both. The clock can be filtered to remove spiking edges.